

**09/759,018**

**Patent**  
**IBM Docket No. FIS920000310US1**

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**In the United States Patent and Trademark Office**

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**Date:** Herewith  
**In re Application of:** Eric V. Kline **Filed:** 01/12/01  
**For:** COMPOSITION AND METHOD FOR CONTAINING METAL  
IONS IN ELECTRONIC DEVICES  
**Serial Number:** 09/759,018 **Confirmation No.** 1799  
**Art Unit:** 2841 **Examiner:** PATEL,  
ISHWARBHAI

**SUPPLEMENTAL APPEAL BRIEF**

Hon. Commissioner of Patents and Trademarks  
P. O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

On April 27, 2006, Appellants appealed from a decision of the Examiner finally rejecting claims 4 to 13. Simultaneously, Appellants filed a Pre-Appeal Brief Request For Review followed by an Appeal Brief. Subsequently, the Examiner issued a second Final Rejection. What follows is Appellants Appeal Brief as required by 37 CFR §41.37. A separate Notice of Appeal will be filed on even date herewith.

**I. Real Party in Interest**

The International Business Machines Corporation, the assignee of the instant application, is

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the real party in interest in this Appeal.

## **II. Related Appeals and Interferences**

There are no appeals, interferences or judicial proceedings related to the instant application or to the appeal of the instant application.

## **III. Status of Claims**

Claims 4 to 13 are pending in this appeal and all of claims 4 to 13 have been finally rejected. Claims 1 to 3 and 14 to 37 have been withdrawn from consideration pursuant to a restriction requirement. No claims are allowed.

A listing of the claims involved in the appeal (claims 4 to 13) can found in the Claims Appendix.

## **IV. Status of Amendments**

No amendment was filed subsequent to the first Final Office Action, mailed January 27, 2006, or the second Final Office Action, mailed October 31, 2006, of the instant application.

After the first Final Rejection, Appellants filed a Pre-Appeal Brief Request For Review. The Panel Decision indicated that there is at least one actual issue for appeal and did not otherwise make a decision. Subsequently, Appellants filed their Appeal Brief on August

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11, 2006. Thereafter, the Examiner issued the second Final Rejection because "there is a great deal of confusion in understanding the previous final action". The present Supplemental Appeal Brief is in response to the second Final Rejection. Appellants will show that the second Final Rejection is still confusing and insufficient as a matter of law to anticipate or render obvious Appellants' claims.

**V. Summary of Claimed Subject Matter**

The present application relates to a method for containing metal ions in electronic devices which utilizes an immobile chelating agent. Conventional electronic devices use metal solders to interconnect electronic components. Such solders typically contain lead and tin. When electronic devices are discarded, the lead and tin can leach from the solder and contaminate the ground water. Merely capturing the lead and tin by a suitable chemical agent such as a chelating agent is not an entirely satisfactory solution since the chelating agent and captured lead and tin may together wash into the ground water. Appellants have proposed a solution in which the chelating agent is immobile so once the lead and tin are captured by the chelating agent, they stay put and will not wash into the ground water.

There is only one independent claim. For the convenience of the Board, it is reproduced here as follows:

4. (Previously presented) An electronic device having an integrated circuit with a composition for containing metal ions, said composition comprising:

a matrix material;

a polymer which serves as an insoluble and immobile phase in said matrix material; and  
a chelating agent which is bonded to said insoluble and immobile phase.

According to the invention, there is a composition 100 for containing metal ions (specification, page 6, line 10; Figure 1). The composition 100 comprises a matrix material, shown in Figure 1 but not separately numbered. As an example of a matrix material, there is shown a conventional encapsulant 410 in Figure 4 (specification page 8, lines 19-23 to page 9, lines 1-4). The inventive composition 100 further comprises a polymer which serves as an insoluble and immobile phase in the matrix material. Figure 1 illustrates "a very high molecular weight insoluble and immobile particle 110" (specification page 6, lines 10-11). Original claim 15 recited "a polymer which serves as an insoluble and immobile phase" which was inserted into claim 4 in place of "a very high molecular weight insoluble and immobile particle 110". The specification (page 6, lines 7-12) was amended accordingly. The inventive composition lastly comprises a chelating agent 120 bonded to the insoluble and immobile phase (specification page 6, line 11; Figure 1).

That the inventive composition 100 can be in an electronic device is described generally at page 8, lines 8-11 and shown in Figures 3 to 9 (specification pages 8-12) for various embodiments.

## **VI. Grounds Of Rejection**

A. Claims 4 and 5 have been rejected by the Examiner under 35 USC §102(b) as being anticipated by Berger U.S. Patent 4,030,948 (hereafter "Berger").

B. Claims 4 to 9 have been rejected by the Examiner under 35 USC §103(a) as being

unpatentable over Raiser et al. U.S. Patent 6,700,209 (hereafter "Raiser") in view of Berger.

C. Claims 11 to 13 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Raiser and Berger and further in view of Ikeda et al. U.S. Patent 5,973,930 (hereafter "Ikeda").

Certain claim objections were made with respect to claims 9 and 12 and those will be discussed below with the rejections of claims 9 and 12.

## **VII. Argument**

The Examiner has failed to establish a *prima facie* case in support of the existing §102 and §103 rejections for the reasons that (i) Berger alone does not show, and Raiser in view of Berger do not teach "a matrix material and a polymer which serves an insoluble and immobile particle phase in said matrix material" as claimed in claim 4, (ii) Berger alone does not show, and Raiser in view of Berger, do not teach "a chelating agent which is bonded to said insoluble and immobile phase" as claimed in claim 4, (iii) Raiser in view of Berger do not teach "wherein said package comprises an organic package and wherein said composition is said organic package" as claimed in claim 9, and (iv) Raiser in view of Berger and Ikeda do not teach "wherein said composition is said printed circuit board" as claimed in claim 12. Each of these will be discussed separately.

A. **Claims 4 and 5 have been rejected by the Examiner under 35 USC §102(b) as being anticipated by Berger U.S. Patent 4,030,948 (hereafter "Berger").**

**(i) Patentability of Claim 4**

Claim 4 recites a matrix material, a polymer which serves as an insoluble and immobile phase in the matrix material and a chelating agent bonded to the insoluble and immobile phase. As taught in Appellants' specification, the chelating agent is bonded to the insoluble and immobile phase which is included in a matrix material. This matrix material may be, for example, a coating, encapsulant, underfill or even an organic package. An element of Appellants' invention is the bonding of the chelating agent to the insoluble and immobile phase so that if the matrix is attacked and leached out by the environment, the chelating agent bonded to the insoluble and immobile phase remains to complex with metal ions that may leach out of metal sources within the electronic device.

Berger teaches a coating which is admixed with a chelating agent. There is no disclosure in Berger for a matrix material containing a chelating agent bonded to an insoluble and immobile phase.

The Examiner in the first Final Office Action states that this element (i.e., "a chelating agent which is bonded to said insoluble and immobile phase") is shown or taught by Berger wherein the immobile phase, supposedly polyimide particles, are in a matrix, also supposedly polyimide. This poorly formulated rationale in the first Final Office Action does not show or teach the above element because there is no immobile phase in a matrix. That is, polyimide can only be soluble within polyimide and thus is not insoluble and immobile. During an interview with the Examiner on April 7, 2006, however, it was determined that what the Examiner actually meant (but never stated in the first Final Office Action) was that the filler particles noted at column 9, lines 33-37, are supposedly the immobile phase. It should be noted that only one of these particles is a polymer and there is no indication in Berger that these particles are insoluble and immobile in the polyimide matrix.

Berger does teach a composition capable of being "...modified with chelating materials admixed therewith or chemically bonded thereto." (col. 4, lines 6-9) Appellants further learned during the interview that it is the Examiner's opinion that chelating agents in the composition of polyimide plus filler material allegedly show or teach the above claim element notwithstanding that there is no disclosure or teaching in Berger that (i) the chelating agents are actually bonded to the filler particles and (ii) the filler particles are an insoluble and immobile phase.

In the second Final Office Action, the Examiner states that the composition of the electronic device comprises "a matrix material (composition, column 34, line 34-35); a polymer which serves as an insoluble and an immobile phase in said matrix material (polyimide particles in the composition are immobile in said composition as the composition is stable with those particles in the composition); and a chelating agent...".

It is to be noted first, that the matrix material in the Examiner's rejection is unspecified and second, that the reference to "(composition, column 34, line 34-35)" must be incorrect since there is no column 34 in the patent. It is possible that the Examiner meant column 4 of Berger since lines 34-35 of Berger reference a "silicon containing polyimide composition".

It is submitted that the Examiner's position is erroneous. For anticipation, each and every element of the claim must be taught. "Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." W.L. Gore & Assocs. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303,313 (Fed. Cir. 1983). If any element is missing, the claim is not anticipated. In re Royka and Martin, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). It is unknown what material the Examiner is claiming as the matrix material and thus, as a matter of law, the Examiner has failed to provide sufficient basis for the anticipation of

claim 4. Assuming *arguendo* that the Examiner is pointing to column 4, lines 34-35 of Berger, the rejection must also fail. From the paragraph bridging columns 4 and 5 of Berger, Berger appears to disclose a copolymer of silicone and polyimide. There do not appear to be any polyimide particles separate from this block copolymer and thus this embodiment of Berger cannot anticipate Appellants' claim 4 which requires a matrix material and a polymer which serves as an insoluble and immobile particle phase in said matrix material. Claim 4 further requires "a chelating agent which is bonded to said insoluble and immobile phase". As there is no disclosure in this embodiment of Berger to indicate that there are any polymer particles, there can be no disclosure in Berger that the absent polymer particles are insoluble and immobile in the matrix. Assuming *arguendo* that the polyimide in the copolymer can somehow constitute particles as required by claim 4, there is no disclosure in Berger that the chelating agent is bonded to the polyimide and there is no disclosure that the polyimide is insoluble and immobile in the matrix. Claim 4, therefore, must be deemed to be not anticipated by Berger.

**B. Claims 4 to 9 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Raiser et al. U.S. Patent 6,700,209 (hereafter "Raiser") in view of Berger.**

**(i) Patentability of Claim 4**

The obviousness rejection of claim 4 as being unpatentable over Raiser in view of Berger is deficient for the same reasons that the anticipation rejection of claim 4 is deficient. The Examiner has failed to state a *prima facie* case of obviousness.

"To establish *prima facie* obviousness of a claimed invention, all the claim limitations



must be taught or suggested by the prior art." MPEP §2143.03. "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Raiser merely discloses an electronic device and cannot otherwise supply the deficiencies of Berger. Berger is deficient at least in not teaching "a chelating agent which is bonded to said insoluble and immobile phase" as claimed in claim 4.

As noted above, the rationale of the Examiner in the second Final Office Action was poorly stated but, as best understood, the Examiner is arguing that the polyimide particles are the immobile phase claimed by Appellants. Again, in the embodiment of Berger possibly pointed to by the Examiner, there do not appear to be any polyimide particles but rather polyimide as part of a silicone and polyimide copolymer.

Assuming *arguendo* that the polyimide of the silicone polyimide copolymer can somehow constitute polyimide particles, there is no teaching in Berger that the polymer particles are insoluble and immobile in the matrix or that the chelating agent is bonded to the polymer particles or, for that matter, that there is any insoluble and immobile phase at all. As noted above, there is disclosure in Berger that the chelating agent may be admixed in the composition or chemically bonded thereto. However, there is no teaching that the chelating agent is added when there are polymer materials and, more importantly, there is no teaching to add the chelating agent so that it will bond to the polymer particles and, most importantly, there is no teaching that the polymer particles are an insoluble and immobile phase. It is equally likely that the chelating agent could be bonded to the matrix material according to the teaching of Berger.

It is a requirement of Appellants' invention that the chelating agent be bonded to the insoluble and immobile particles so that should the matrix be attacked by the environment, the matrix is partially dissolved but the chelating agent remains since it is bonded to the insoluble and immobile particles. In Berger, the coating already is impervious to moisture (col. 3, lines 58-59) so there is no motivation to bond the chelating agent to the polymer particles (assuming *arguendo* that there are polymer particles which are insoluble and immobile in the matrix). It follows that since the Berger matrix can be impermeable to moisture, Berger does not recognize the problem of the dissolution of the matrix or the solution to the problem and thus the need to have a chelating agent bonded to insoluble and immobile particles. "The mere fact that the prior art could be modified would not have made the modification obvious unless the prior art suggested the desirability of the modification." In re Gordon, 733 F.2d 900, 902; 221 USPQ 1125, 1127 (Fed. Cir. 1984). Berger could be modified to bond the chelating agent to an insoluble and immobile phase (again, assuming *arguendo* that Berger discloses such an insoluble and immobile phase) but since the Berger coating is impervious to moisture, there is no need to do so and thus there is nothing in Berger to suggest the desirability of doing so. Accordingly, Berger does not teach this element of Appellants' invention and Raiser cannot supply the deficiencies of Berger.

For all of the foregoing reasons, it is submitted that the combination of Raiser and Berger cannot render obvious Appellants' claim 4.

**(ii) Patentability of Claim 9**

It is not clear why the Examiner is objecting to the wording of claim 9. It was thought that in the interview of April 7, 2006, with the Examiner, the Examiner's concern with the wording of claim 9 was cleared up. Evidently not. In any event, Appellants assert that the

wording is sufficient as written and does not need correction. The novel composition of the present invention is the organic package and this is clearly recited as claim 9.

Turning to the rejection of claim 9, Raiser in view of Berger do not teach "wherein said package comprises an organic package and wherein said composition is said organic package" [emphasis added] as claimed in claim 9.

In the rejection of claim 9, the Examiner stated in the Final Office Action that Berger in figure 5 discloses a substrate made of resin and the composition 160 (containing the chelating agent) is contained within the package. Raiser clearly does not teach the above element as Raiser merely discloses an electronic device.

Appellants submit that the Examiner's position is erroneous. The disclosure in Berger is for a coating 160 which is on the organic package. Claim 9 requires that "said composition is said organic package" not that the composition is on the organic package. While the Examiner may argue that the coating 160 forms a part of the organic package, it is not the organic package per se as claimed by Appellants in claim 9. Therefore, Berger cannot teach this element of Appellants' claim 9 and since Raiser cannot otherwise supply the deficiencies of Berger, the Examiner is deemed to have failed to state a *prima facie* case of obviousness with respect to claim 9.

**C. Claims 11 to 13 have been rejected by the Examiner under 35 USC §103(a) as being unpatentable over Raiser and Berger and further in view of Ikeda et al. U.S. Patent 5,973,930 (hereafter "Ikeda").**

**(i) Patentability of Claim 12**

Again, it is not clear why the Examiner is objecting to the wording of claim 12. It was thought that in the interview of April 7, 2006, with the Examiner, the Examiner's concern with the wording of claim 12 was cleared up. Evidently not. In any event, Appellants assert that the wording is sufficient as written and does not need correction. The novel composition of the present invention is the printed circuit board and this is clearly recited as claim 12.

Turning now to the rejection, Raiser in view of Berger and Ikeda do not teach "wherein said composition is said printed circuit board" as claimed in claim 12.

In the Final Office Action, the Examiner applied the same rationale for the rejection of claim 12 as was applied for the rejection of claim 9. Raiser and Ikeda clearly do not teach the above element as Raiser merely teaches an electronic device and Ikeda merely teaches an electronic package with underfill.

Appellants' remarks applicable to the patentability of claim 9 are equally applicable to the rejection of claim 12. That is, the disclosure in Berger is for a coating 160 on the organic package but Berger does not teach "wherein said composition is said printed circuit board". Accordingly, Berger cannot teach this element of Applicants' claim 12 and since Raiser and Ikeda cannot supply the deficiencies of Berger, the Examiner is deemed to have failed to state a *prima facie* case of obviousness with respect to claim 12.

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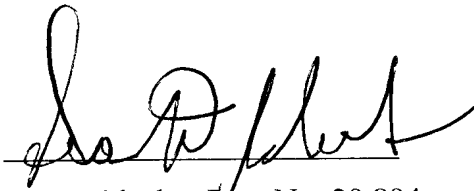
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**VIII. Summary**

In view of all of the preceding remarks, it is submitted that claims 4 to 13 are in condition for allowance, that the Examiner's various rejections of claims 4 to 13 are erroneous and reversal of the Examiner's decisions is respectfully requested.

Respectfully Submitted,

Eric V. Kline

A handwritten signature in black ink, appearing to read 'Ira D. Blecker', written over a horizontal line.

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**CLAIMS APPENDIX**

4. An electronic device having an integrated circuit with a composition for containing metal ions, said composition comprising:

- a matrix material;
- a polymer which serves as an insoluble and immobile particle phase in said matrix material; and
- a chelating agent which is bonded to said insoluble and immobile particle phase.

5. The electronic device according to claim 4, wherein said composition is a scratch coat covering an active surface of said integrated circuit.

6. The electronic device according to claim 4, further comprising:

- a package, to which said integrated circuit is bonded.

7. The electronic device according to claim 6, wherein said composition is an encapsulant which is deposited over substantially an entire surface of said integrated circuit and between said integrated circuit and said package.

8. The electronic device according to claim 6, wherein said composition is an underfill which is deposited between said integrated circuit and said package.

9. The electronic device according to claim 6, wherein said package comprises an organic package and wherein said composition is said organic package.

10. The electronic device according to claim 6, further comprising:

a printed circuit board to which said package is bonded.

11. The electronic device according to claim 10, wherein said composition is an underfill which is deposited between said package and said printed circuit board.

12. The electronic device according to claim 10, wherein said composition is said printed circuit board.

13. The electronic device according to claim 10, wherein said composition is a conformal coating which is deposited over said integrated circuit, said package and said printed board.

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**EVIDENCE APPENDIX**



# United States Patent [19]

Berger

[11] 4,030,948

[45] June 21, 1977

[54] POLYIMIDE CONTAINING SILICONES AS  
PROTECTIVE COATING ON  
SEMICONDUCTOR DEVICE

[76] Inventor: Abe Berger, 1504 Barclay Place,  
Schenectady, N.Y. 12309

[22] Filed: July 21, 1975

[21] Appl. No.: 597,971

[52] U.S. Cl. .... 148/33.3; 148/186

[51] Int. Cl.<sup>2</sup> .... H01L 21/56

[58] Field of Search .... 148/33.3

[56]

## References Cited

### UNITED STATES PATENTS

3,615,913 10/1971 Shaw ..... 148/33.3  
3,684,592 8/1972 Chang et al. .... 148/33.3

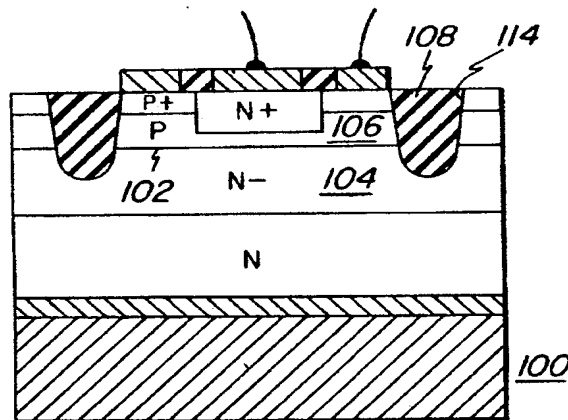
Primary Examiner—L. Dewayne Rutledge  
Assistant Examiner—J. M. Davis

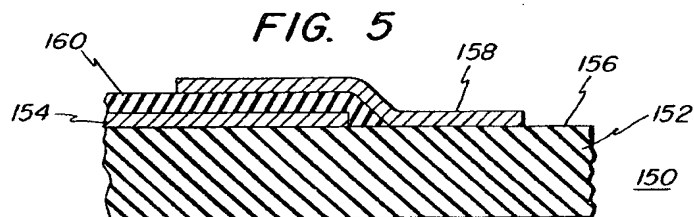
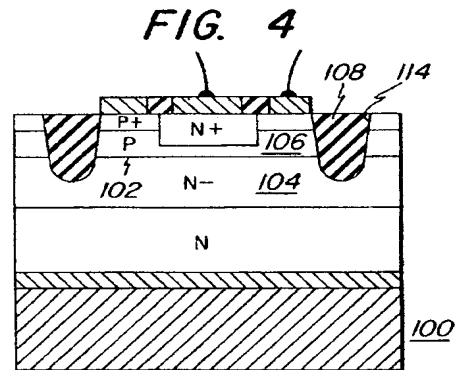
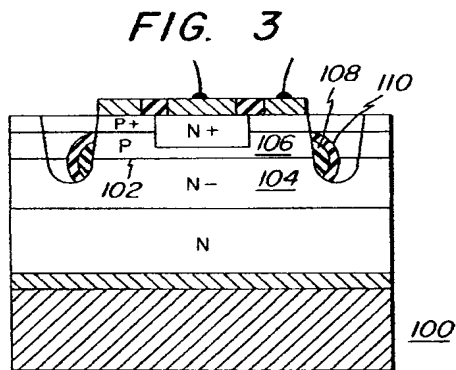
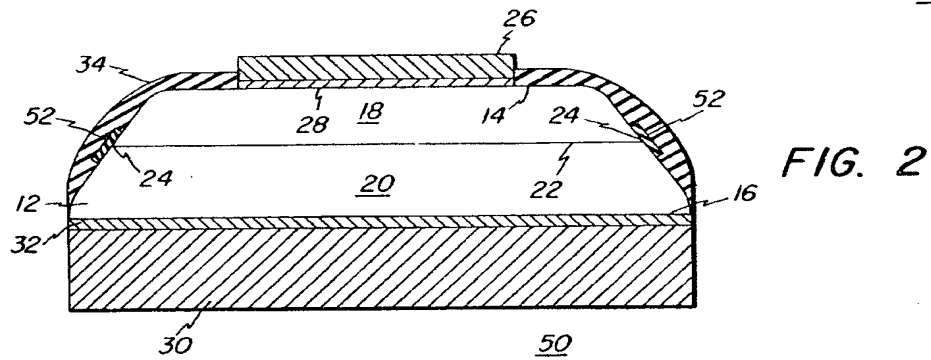
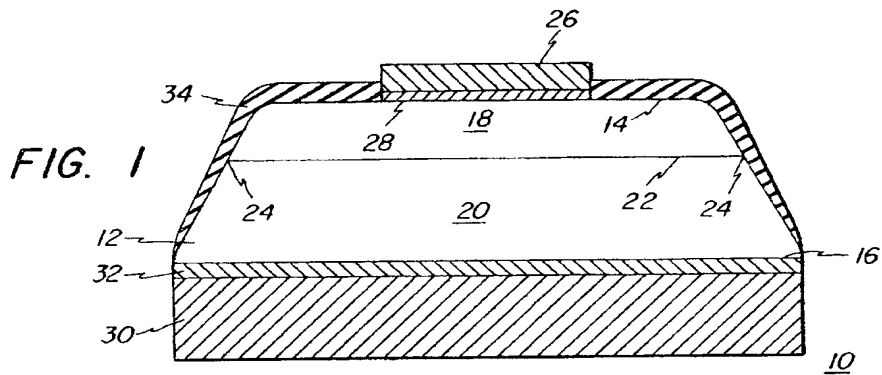
[57]

## ABSTRACT

A copolymer which is the reaction product of a tetracarboxylic acid dianhydride, and organic diamine and a di(aminoalkyl) poly siloxane where the di(aminoalkyl) poly siloxane constitutes 18 – 45 mole percent of the total amine requirement of the polymer and is applicable as a conformal protective coating for electronic devices.

9 Claims, 5 Drawing Figures





# POLYIMIDE CONTAINING SILICONES AS PROTECTIVE COATING ON SEMICONDUCTOR DEVICE

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

This invention relates to conformal protective coatings for electronic devices and, in particular, to a copolymer which is a reaction product of a tetracarboxylic acid dianhydride, a diamine and a di(aminoalkyl)-siloxane.

### 2. Description of the Prior Art

A semiconductor device which exhibits an undesirable resistance to reverse biasing breakdown often has been found to have detrimental leakage currents existing on selected surface areas during operation of the device. The leakage currents arise from the mobility of ions which are formed from ions of adsorbed molecules.

Heretofore, prior art methods to correct such deficiencies provided a means for protecting selected surface areas of electrical devices, in particular, exposed end portions of P-N junctions of a semiconductor device, with an electrically insulating material such, for example, as silicon oxide, silicon nitride, aluminum nitride and the like. Such materials are provided as a thin layer of a coating material on the selected surface area and have virtually no resistance to mechanical abrasion and require relatively expensive processing techniques and equipment. In many instances a second, and thicker, layer of coating material is disposed on the layer of electrically insulating material to provide a suitable abrasive protective means therefor. Silicone varnishes, rubbers, resins and the like are employed as the overcoating material but often lack suitable physical characteristics. Often these silicone materials require two components which must be mixed together, a catalyst to aid in curing, extensive curing times up to 24 hours and more, and chelating agents admixed therein.

Improvements have been made such, for example, as provided by Shaw in his U.S. Pat. No. 3,615,913. However, the improved material lacks desirable adhesion and electrical properties required for some electronic device applications.

In a series of U.S. patents including U.S. Pat. Nos. 3,325,450 and 3,740,305, Holub teaches a Terpolymer System consisting of a Diamino Siloxane, an organic diamine and a Tetracarboxylic Acid Dianhydride are disclosed. In these patents the combinations of the Diamino Siloxanes with the organic diamine varied between the two extremes in conjunction with molar quantities of Tetracarboxylic Acid Dianhydride. It is not apparent from the teachings of these patents that any specific combination of components would be more effective coating materials over and beyond their direct relationship to either the 100% polyimide or 100% polysiloxane terminal component.

It is an object of this invention to provide a new and improved conformal coating suitable for use on electronic components.

Another object of this invention is to provide a polyimide-siloxane copolymer material for use as a conformal coating on electronic components wherein the copolymer contains from 18 to 45 mole percent of the silicone diamine.

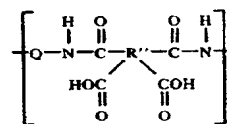
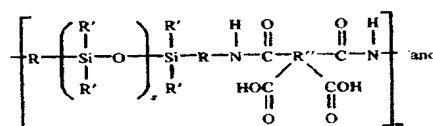
Another object of this invention is to provide a copolymer which is a reaction product of a tetracarbox-

ylic acid dianhydride, a diamine and a di(aminoalkyl)siloxane.

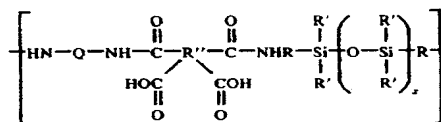
Other objects of this invention will, in part, be obvious and will, in part, appear hereinafter.

## Summary of the Invention

In accordance with the teachings of this invention, there is provided a reaction product of a tetracarboxylic acid dianhydride, a diamine and a di(aminoalkyl) polysiloxane wherein the polysiloxane diamine constitutes from 18 to 45 mole percent of the total diamines in the copolymer. The copolymer has recurring structural units of a block copolymer of the formulas:



and a random polymer of the formula:



wherein:

R is a divalent hydrocarbon radical;

R' is a monovalent hydrocarbon radical wherein each

R' may be the same radical or a different radical from the others;

R'' is a tetravalent organic radical;

Q is a divalent organic radical which is a residue of an organic diamine;

x is an integer having a value of from 1 to 10;

m is an integer greater than 1 and

n is an integer greater than 1.

p is an integer greater or equal to 0.

The ratios of the recurring units designated by m, n, and p are such that the quantity of silicone diamine in the total polymer constitutes from 18 to 45 mole percent of the total diamines in the polymer. The material is particularly suitable for the application of conformal coatings thereto to improve the operating characteristics of semiconductor and other electrical devices. The copolymer is a suitable conformable protective and dielectric coating for electronic devices such, for example, as semiconductor devices having at least one P-N junction exposed in a surface area thereof, thick and thin films circuits, printed circuits, faces of cathode ray vacuum tubes, high voltage leads and connections to cathode ray vacuum tubes and the like.

## DESCRIPTION OF THE DRAWINGS

FIGS. 1 through 5 are views, in cross-section of electronic devices made in accordance with the teachings of the invention.

## DESCRIPTION OF THE INVENTION

Referring now to FIG. 1, there is shown a semiconductor element 10 embodying any one of the novel conformal coating materials of this invention. The element 10 is comprised of a body 12 of single crystal semiconductor material. A suitable semiconductor material for comprising the body 12 may be silicon, silicon carbide, germanium, gallium arsenide, a compound of a Group III element and a Group V element of the Periodic Table or a compound of a Group II element and a Group VI element of the Periodic Table. In order to describe the invention more fully, and for purposes of illustration only, the body 12 is said to be comprised of silicon semiconductor material.

The body 12 is prepared by suitable means, such, for example, as by polishing and lapping to parallelism two major opposed surfaces 14 and 16. The body 12 has two, or more, regions 18 and 20 of alternate and opposite type conductivity. A P-N junction 22 is formed by the contiguous surfaces of each abutting pair of regions of opposite type conductivity. End portions 24 of the P-N junction 22 are exposed in the surface area of the body 12.

A first electrical contact 26 is affixed to, and is in an electrically conductive relationship with, the region 18 by a layer 28 of a suitable electrically conductive solder material. A second electrically conductive contact 30 is affixed to the bottom surface 16 of the body 12 by a layer 32 of a suitable electrically conductive solder material. The electrical contacts 26 and 30 provide means for electrically connecting the element 10 into electrical circuitry. When required, the contacts 26 and 30 should exhibit good thermal conductivity properties as well in order to dissipate any heat generated in the body 12 particularly in high voltage, high ampera power devices.

One or more layers 34, as required, of an electrically insulating coating is disposed on at least selected surface areas 36 of the body 12 wherein the end portions 24 or P-N junctions 22 are exposed thereat. Preferably, it is desirable to apply the material layer 34 to all exposed surface areas of the body 12. The material of the layer 34 comprises one of the novel conformal coating materials to be described heretofore.

A conformal protective coating material suitable for use with electric devices must have several desirable physical characteristics. The material must be one which can easily be applied and cured in place. The material must not degrade, but should preferably enhance, the electrical characteristics of the device to which it is applied. The material should adhere very tenaciously to the surface to which it is applied to prevent migration of ions on the surface of the device, particularly when employed with semiconductor devices, and should not release any materials during a curing cycle which are deleterious to the operating characteristics of the device. The coating should be impermeable to moisture and exhibit good abrasion resistance when cured to protect the surfaces to which the coating is applied.

The material should also be capable of being applied in multiple layers to provide a thick coating when required. Therefore, the material must be able to bond well to itself. Should the electronic device be employed in circuitry where corona is a problem, the material must be able to exhibit good corona resistance when cured.

When a material is not capable of inherently exhibiting the above desired characteristics, it must be capable of being modified to achieve the desired end result. Often times stray alkali and heavy metal ions cause undesirable degradation of electrical properties of semiconductor devices. Therefore, the material of the coating must be capable of being modified with chelating materials admixed therewith or chemically bonded thereto. Ease of application to the surface to be protected and reasonably short curing times must still be retained. This is particularly true when the coating material is employed in commercial manufacturing of mass produced electronic devices.

Although the coating material when cured may be opaque, it is more desirable to have the material highly translucent. Such a material, if retaining the other desirable characteristics, would be invaluable for photovoltaic devices. Particularly, it would be desirable to a light emitting diode to the surface of another semiconductor device and be capable of turning the device "on" and "off" in response to the operation of the light emitting diode.

Normally the presence of alkali metal contaminants present either on the surface of devices to be coated, or in the coating materials, creates surface current leakage in the device that limits their useful operation. To circumvent these difficulties, chelating agents such as alizirin, catechol and the like are mechanically admixed with the coating materials before being applied to, and cured on the device surface. However nonuniformity of mixtures result in hazy films, loss of adhesion, etc. making alternate treatments highly desirable for prevention of surface leakage of devices.

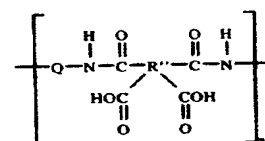
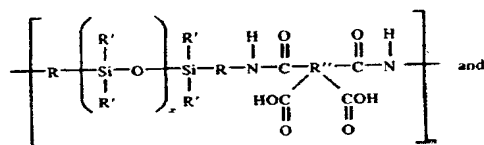
I have discovered that silicone containing polyimide compositions wherein the silicone diamine constitutes from 18 to 45 mole percent of the total amine present therein. Preferably from approximately 28 to about 32 mole percent of the total amine in the material product produces coatings which upon curing on the surface of the semiconductor device results in very low leakage current so that additional additives are not required. Furthermore, if the silicone diamine molar ratios fall outside the range of from 18 to 45 mole percent leakage currents increase considerably so that additives once again become a necessity. The resulting leakages are still unacceptable even when such additives are used.

The beneficial effect of low leakage current within the scope of my invention is achieved without loss of other desirable properties such, for example, as adhesion, anticorona properties, high temperature properties and the like of the resulting coating material. Unexpectedly, the narrow range of silicone diamine compositions of this invention achieve such beneficial effects.

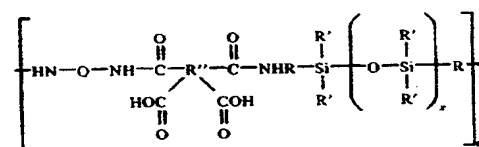
It is not obvious to those skilled in the art that such a beneficial effect would be obtained by the use of the narrow ranges of silicone compositions described above. Other beneficial results derived from the use of these polymer compositions are as follows: sharp breakdown voltage (approaching theoretical performance of devices) increase adhesion to a wide variety of substrates, extremely high temperature performance outstanding barrier properties to moisture and other gases, unusually high corona resistance, strong coherent films resistant to scratching and marring and the like.

I have discovered that the above described desirable characteristics are achieved by the reaction product of

a tetracarboxylic acid dianhydride, a diamine and a di(aminoalkyl) siloxane. The reaction product is a copolymer which has, depending on the modes of mixtures employed, the recurring structural units of a block copolymer of the formulas:



and a random polymer of the formula:



wherein:

R is a divalent hydrocarbon radical;

R' is a monovalent hydrocarbon radical wherein each R' may be the same radical or a different radical from the others;

R'' is a tetravalent organic radical;

Q is a divalent organic radical which is a residue of an organic diamine

x is an integer having a value of from 1 to 10;

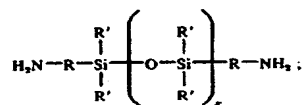
m is an integer greater than 1, and

n is an integer greater than 1.

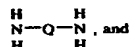
p is an integer greater than or equal to 0.

The recurring units designated by m, n, and p are such that the quantity of silicone diamine in the total polymer constitutes from 18 to 45 mole percent of the total diamines the polymer.

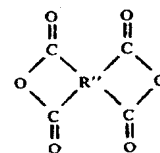
The copolymers of the invention are prepared by reacting a mixture of chemical ingredients which is composed of a di(aminoalkyl) polysiloxane of the general formula:



a diamino compound having the general formula:

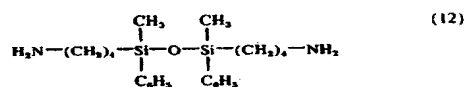
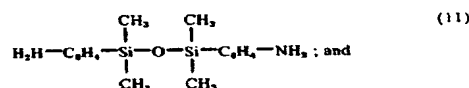
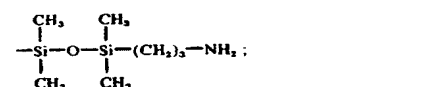
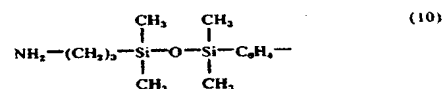
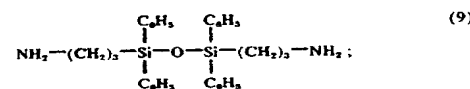
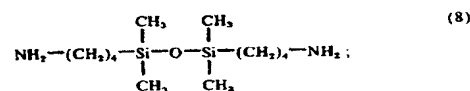
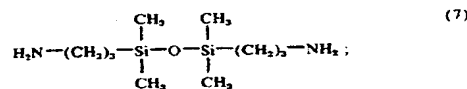


a tetracarboxylic acid dianhydride having the formula:



wherein R, R', R'', Q and x have the same meanings as described heretofore.

The di(aminoalkyl) polysiloxanes of formula (4) which may be used in the practice of the present invention are limited in that when x is 10 or more they lose their adhesive properties and, consequently, x preferably equals 1-9. The following formulas are descriptive of those di(aminoalkyl) polysiloxane compounds which may be included in the reactive ingredients to make the new copolymer:



Other suitable di(aminoalkyl) siloxane compounds may also be included as one of the reaction ingredients.

Diamines of formula (5) are known in the prior art and many of them are commercially available. Suitable diamines for use as one of the reaction mixture are as follows:

m-phenylenediamine;

p-phenylenediamine;

4,4'-diaminodiphenylpropane;

4,4'-diaminodiphenylmethane; benzidine;

4,4'-diaminodiphenyl sulfide;

4,4'-diaminodiphenyl sulfone;

4,4'-diaminodiphenyl ether;

1,5-diaminonaphthalene;

3,3'-dimethylbenzidine;

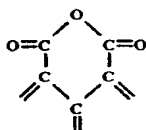
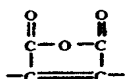
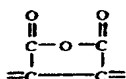
3,3'-dimethoxybenzidine;

2,4-bis(β-amino-t-butyl)toluene;

bis(p-β-amino-t-butylphenyl)ether;  
 bis(p-β-methyl-o-aminopentyl)benzene;  
 1,3-diamino-4-isopropylbenzene;  
 1,2-bis(3-aminopropoxy)ethane;  
 m-xylylenediamine;  
 p-xylylenediamine;  
 bis(4-aminocyclohexyl)methane;  
 decamethylenediamine;  
 3-methylheptamethylenediamine;  
 4,4-dimethylheptamethylenediamine;  
 2,11-dodecanediamine;  
 2,2-dimethylpropylenediamine;  
 octamethylenediamine;  
 3-methoxyhexamethylenediamine;  
 2,5-dimethylhexamethylenediamine;  
 2,5-dimethylheptamethylenediamine;  
 3-methylheptamethylenediamine;  
 5-methylnonamethylenediamine;  
 1,4-cyclohexanediamine;  
 1,12-octadecanediamine;  
 bis(3-aminopropyl)sulfide;  
 N-methyl-bis(3-aminopropyl)amine;  
 hexamethylenediamine;  
 heptamethylenediamine;  
 nonamethylenediamine;  
 In addition, mixtures of the above diamines may also be employed.

It should be noted that these diamines are given merely for the purpose of illustration and are not considered to be all inclusive. Other diamines not mentioned will readily be apparent to those skilled in the art.

The tetracarboxylic acid dianhydrides of formula (6) may be derived from, or contain, either an aromatic, acrylic or cyclic aliphatic carbon radical. Therefore, the tetracarboxylic acid dianhydrides of formula (6) may further be defined in that R'' is a tetravalent radical derived from, or containing, an aromatic radical containing at least 6 carbon atoms characterized by benzenoid unsaturation, wherein each of the 4 carbonyl groups of the dianhydride are attached to a separate carbon atom in the tetravalent radical. The carbonyl groups are in pairs and the carbonyl radicals in each pair are attached to adjacent carbon atoms of the R'' radical or to carbon atoms in the R'' radical at most one carbon atom removed, to provide a 5-membered or 6-membered ring of one of the following formulas:



Illustrative of such tetracarboxylic acid associated with an aromatic carbon radical dianhydrides which are suitable for use in the present invention, along with

their commonly known designation in parentheses, are the following:

- pyromellitic dianhydride (PMDA);
- 2,3,6,7-naphthalene tetracarboxylic dianhydride;
- 5 3,3',4,4'-diphenyl tetracarboxylic acid dianhydride;
- 1,2,5,6-naphthalene tetracarboxylic acid dianhydride;
- 2,2',3,3'-diphenyl tetracarboxylic acid dianhydride;
- 2,2-bis(3,4-dicarboxyphenyl)propane dianhydride;
- 2,2-bis(4,4'-di[3,4-dicarboxyphenoxy]phenyl)propane dianhydride;
- 10 bis(3,4-dicarboxyphenyl) sulfone dianhydride;
- benzophenone tetracarboxylic acid dianhydride (BPDA);
- perylene-1,2,7,8-tetracarboxylic acid dianhydride;
- 15 bis(3,4-dicarboxyphenyl)ether dianhydride, and
- bis(3,4-dicarboxyphenyl) methane dianhydride;

Alternately acyclic or cyclic aliphatic anhydrides such, for example, as cyclopentane tetracarboxylic acid dianhydride, cyclohexane tetracarboxylic acid dianhydride, butane tetracarboxylic acid dianhydride, and the like, are also suitable for use in the present invention.

The copolymers materials of this invention are soluble in, or may be diluted by, suitable materials for the application of the material to surfaces of electronic devices. The application of the material to the surface may be painting on the material, spraying, dipping and the like. Any means of application may be used which will ensure the complete coverage of the surface to which it is applied. Suitable solvents and diluents are, for example, N-methylpyrrolidone, N,N-dimethylacetamide, N,N-dimethylformamide, tetramethylurea, hexamethylphosphorous triamide, dimethyl-sulfoxide, and the like.

The copolymer materials of this invention are suitable for use on surfaces of selected, glass, ceramic, organic and inorganic materials and the like. Suitable organic material surfaces are those of such, for example, as thermoplastic materials. Suitable thermoplastic materials are such, for example, as a polyimide, a polyester, a polycarbonate, a polyamide and the like. The novel copolymers of this invention also show excellent bonding to fibrous materials comprising such, for example, as those consisting of glass, boron, quartz, carbon and the like, as well as to cloths embodying the same materials. The novel copolymer materials are also suitable for achieving a good adhesion bond to finely divided materials such, for example, as metals, carbon, quartz, and ceramics such, for example, as alumina, benzene and the like.

(13) 50 After application of the conformal coating material to the surface area of the body 12, it is cured in situ. A recommended curing cycle is to heat the element and applied coating material slowly to a temperature just below the boiling point of the solvent in the coating. A (14) 55 period of about 30 minutes at this temperature is preferred in order to volatilize the solvent as much as possible without causing the formation of bubbles in the coating material. The temperature may be then increased approximately 50° C to reach a level which is (15) 60 above the boiling point of the solvent. It is held at this higher temperature for about 30 minutes to eliminate substantially all of the solvent and to increase the imidization of the materials of the coating. A further curing step at an elevated temperature about 50° C higher (16) 65 than before for about 30 minutes is followed by an additional curing step practiced at a temperature of about 50° C higher for sufficient time to complete about a 3 hour curing cycle. This procedure has been

found to be sufficient to produce a very desirable conformable coating for the element 10. A typical curing cycle for the copolymers of this invention is about 30 minutes at  $150^{\circ}\text{C} \pm 10^{\circ}\text{C}$ , about 30 minutes at  $200^{\circ}\text{C} \pm 10^{\circ}\text{C}$ , about 30 minutes at  $250^{\circ}\text{C} \pm 10^{\circ}\text{C}$  and  $300^{\circ}\text{C} \pm 10^{\circ}\text{C}$  for the remainder of a 3 hour curing cycle.

When cured in situ, the conformal coating comprises a polyimide of the structure described heretofore. The layer 34 of cured coating material adheres tenaciously to the silicon surface upon which it is disposed. The cured coating material is impervious to moisture and gases such, for example, as oxygen and nitrogen. The cured material has excellent abrasion resistance properties to protect the element, corona resistance and dielectric strength. The excellent adherence to the surface apparently is responsible for a significant reduction in current leakage on the surface of the body 12 and particularly in the vicinity of the end portions 24 of the P-N junction 22 exposed in the surface of the body 12.

The dielectric strength of the cured material of the layer 34 may be further enhanced by admixing suitable filler materials therein. Preferably, an electrically insulating material having a dielectric constant which is approximately the same as the material of the layer 34 is admixed therein. The filler material is uniformly distributed throughout the coating material as applied. Other materials suitable as a filler material are those materials known to have a relatively good ability to resist electrical conduction although their dielectric constant is higher than that of the material of the layer 34. Suitable electrically insulating filler materials have been found to include aluminum oxide, silicon oxide, glass fibers, boron nitride, quartz, mica, magnesium oxide, activated polytetrafluoroethylene, and the like, in a finely divided, or a pulverized form.

With either a filled, or an unfilled siloxane containing polyimide material, the electrical properties of the element 10 are enhanced. The cured coating material of the layer 34 has an inherent elasticity to withstand repeated cycling from dipping in liquid gases in temperature ranges of approximately  $-100^{\circ}\text{C}$  to heating in a furnace at approximately  $300^{\circ}\text{C}$  and back into a liquid gas for a temperature excursion range of about  $400^{\circ}\text{C}$  or more. Additionally, I have found the cured materials of the layer 34 to withstand short temperature excursions up to about  $400^{\circ}\text{C}$  to  $500^{\circ}\text{C}$  without degradation of the electrical characteristics of the element 10.

The material of the layer 34 may also be applied over electrically insulating layers of silicon oxide, silicon nitride, aluminum nitride and the like. Referring now to FIG. 2, there is shown an element 50 which is an alternate embodiment of the element 10. All items denoted by the same reference numbers are the same, and function in the same manner, as the corresponding item in FIG. 1.

The element 10 is modified by the deposition of a layer 52 of an electrically insulating material on at least the exposed end portions of the P-N junction 22 and the adjacent surface areas of the body 12. The layer 52 minimizes the current leakage across the exposed end portions. The material of the layer 52 is one selected from the group consisting of silicon oxide, silicon nitride and aluminum nitride. One of more layers 34 of a filled or an unfilled coating material of this invention is disposed over at least the layer 52 to protect the integrity of the electrical properties of the element 50.

The novel siloxane containing polyimides of this invention are also suitable, because of their ease of application and curing, as a protective coating for semiconductor elements embodying a "moat" type isolation groove. Moats or grooves are suitable for use in high power semiconductor elements wherein current leakage which occurs at exposed end portions of P-N junctions must be controlled. As shown with reference to FIG. 3, a high-speed power transistor 100, the end portions of P-N junction 102 formed by the abutting surfaces of the N-region 104 and the P-region 106 must be protected by a suitable dielectric protective coating.

The protective coating may comprise one or two layers 108 and 110 of suitable material which are the same as, or different from, each other. The material of the layer, 108 and 110 may be any of the materials described heretofore relative to the layer 34 of the elements 10 and 50 of FIGS. 1 and 2 respectively. Additionally, the layer 108 may also comprise one of the electrically insulating materials comprising the layer 52 of the element 50.

Referring now to FIG. 4, the layer 108 of dielectric protective coating material is shown deposited in a moat or groove 114 employed to control leakage across the end portions of the P-N junction 102 exposed therein. Often it is easier to fill the groove by "painting" or by silk-screening and curing in situ.

With reference to FIG. 5, there is shown a portion of a printed circuit board assembly 150. The assembly comprises a board 152 of suitable material such for example as fiberglass, phenolic resin or malamine resin impregnated cloth and the like. A first electrically conductive metal circuit 154 is disposed on a selected portion of the surface 158 of the board 152. A second electrically conductive metal circuit 158 is disposed on another portion of the surface 156 and overlies, in part, a portion of the circuit 154. The material of the circuits 154 and 158 may be of copper, aluminum and the like. A layer 160 of a suitable conformal coating material such, for example, as described with reference to the layer 32 of the elements 10 and 50, described heretofore, is disposed on at least the circuit 154. When cured in situ, the material of the layer 160 shows excellent adherence to the board 152 and the material of the circuit 154. The metal of the layer 158 adheres well to the cured conformal coating material and is electrically isolated thereby from the metal circuit 154.

The following examples are illustrative of the teachings of this invention:

#### EXAMPLE I

##### Polyimide Containing 30 Mole Percent Silicone

A mixture of 163 parts by weight of n-methylpyrrolidone, 13.86 g (0.07 Mole) 4,4'-methylenedianiline, 8.28 g (0.03 mole) 1,3-bis(8-aminobutyl) tetramethyldisiloxane was charged to a reaction flask flushed with nitrogen. The reaction was stirred until a homogeneous mixture was reasonably assured. To the mixture was then added 32.22 (0.1 mole) benzophenone tetracarboxylic acid dianhydride while the mixture was continually agitated. The agitation was continued until a homogeneous viscous fluid was obtained in approximately four hours to assure that the reaction had been completed.

A sample of the fluid was disposed on a surface of a glass slide. Curing was achieved by heating the coated slide for  $\frac{1}{2}$  hour at  $150^{\circ}\text{C} \pm 5^{\circ}$  followed by 10 minutes at

250° C $\pm$ 5° C. The resulting film coating showed excellent adherence to the glass surface and exhibited excellent abrasion resistance when abraded by a spatula.

The coated slide was immersed in boiling water for 8 hours. The coated slide was then removed, cooled to room temperature, and dried. No degradation in adherence or abrasion resistance was observed.

#### EXAMPLE II

##### Polyimide Containing 30 Mole Percent Silicone

A polyimide containing 30 mole percent silicone was prepared in the same manner as in Example I and was applied to the junction of a power transistor and leakage was tested for under reverse bias conditions. An unusually low leakage (less than 1 Nano amp) and a very sharp breakdown voltage was observed.

#### EXAMPLE III

##### Polyimide Containing 10 Mole Percent Silicone at 25% Solid Concentration

A slurry containing 2.76 parts of bis( $\delta$ -aminobutyl) tetramethyldisiloxane and 17.82 parts methylenedianiline in 159 parts by weight of n-methylpyrrolidone was maintained under a nitrogen atmosphere and a temperature of from 0° to 5° C by an ice bath. Vigorous stirring was maintained and 32.2 parts benzophenone tetracarboxylic dianhydride was added. The mixture was stirred vigorously for an additional two hours after the addition. The ice bath was removed and the reaction was allowed to continue, being vigorously stirred overnight (8 hours) at ambient temperature. A clear yellow viscous solution was thus obtained.

A cured film showed marginal adhesion to the surface of a glass slide and under boiling water peeled off after a period of 3 hours.

A sample of the prepared material was coated on an exposed end portion of a P-N junction of a power transistor and tested for surface leakage under reverse bias conditions. The leakage current readings were of the order of from 200 to 300 Nano amps and the results contrasted sharply to those coated with material containing 30 mole percent silicone diamines. The material of this example was not acceptable for semiconductor applications.

#### EXAMPLE IV

##### Polyimide Containing 45 Mole Percent Silicone

As in Example II the combination of 12.42 parts bis( $\delta$ -aminobutyl) tetramethyldisiloxane and 10.89 parts of methylenedianiline in 165 parts of N-Methylpyrrolidone with 32.2 parts benzophenone tetracarboxylic dianhydride with cooling and stirring produced a viscous deep amber fluid.

A sample of the prepared fluid was coated on an exposed end portion of a P-N junction of a power transistor. The applied material was cured by heating the coated device for ½ hour at 150° C $\pm$ 5°, followed by 2 hours at 210° C $\pm$ 5° followed by ½ hour at 250° C $\pm$ 5°. The leakage current under reverse bias conditions was measured. The leakage current was greater than that measured in the example of Group I but was acceptable.

#### EXAMPLE V

##### Polyimide Containing 30 Mole Percent Silicone Derived From Pyromelitic Dianhydride

The procedure of Example I was followed in that to a slurry consisting of 7.44 parts bis( $\delta$ -aminopropyl) tetramethyldisiloxane, 7.56 parts m-Phenylene diamine and 111 parts N-Methylpyrrolidone under N<sub>2</sub> and vigorously stirred with cooling in an ice bath was added 21.8 parts pyromelitic anhydride. Upon complete solution, the ice bath was removed and the clear viscous solution stirred for an additional 6 hours.

A sample of the prepared solution was applied as a coating on an exposed portion of a P-N junction of a power transistor and tested for leakage current under reverse bias conditions. Readings obtained were of the order of 5 Nano amps, again illustrating excellent electrical properties of such coating materials. Excellent adhesion, abrasion resistance and resistance to the eight hour boiling water tests were achieved.

Standard test samples were prepared for each of the above copolymers of the Examples and subjected to standard corona testing as mentioned by the industry.

The prior art copolymer of silicone free polyimides failed after approximately 50 hours average testing time for the samples of the conformal coating material submitted for testing. This indicated that the prior art material was equivalent to mylar for corona resistance.

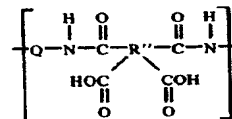
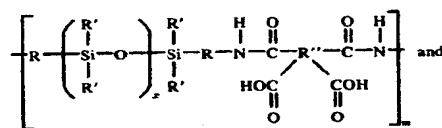
The conformal coating materials of this invention were found to be approximately 40 to about 60 times better than mylar when tested for corona resistance.

What I claim is:

1. A semiconductor element comprised of a body of semiconductor material having at least two regions of opposite-type semiconductivity and a P-N junction disposed between each pair of regions of opposite type semiconductivity:

and end portion of at least one P-N junction exposed at a surface of the body; and

at least one layer of conformal protective coating material disposed on the exposed end portion of the at least one P-N junction, the layer comprising a copolymer which is a reaction product of a tetracarboxylic acid dianhydride, a diamine and a di(aminoalkyl) siloxane, which is a copolymer having recurring structural units of a block copolymer of the formulas:

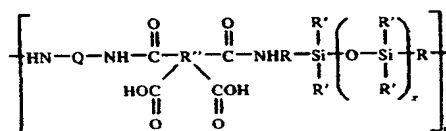


and a random polymer of the formula:



13

-continued



wherein:

R is a divalent hydrocarbon radical;

R' is a monovalent hydrocarbon radical wherein each

R' may be the same radical or a different radical from the others;

R'' is a tetravalent organic radical;

Q is a divalent organic radical which is a residue of an organic diamine;

x is an integer having a value of from 1 to 10;

m is an integer greater than 1 and

n is an integer greater than 1,

p is an integer greater than or equal to 0,

and the recurring units designated by m, n, and p are such that the mole percent of silicone diamine in the total polymer constitutes 18 to 45 mole percent of the total diamines in the copolymer.

2. The semiconductor element of claim 1 wherein the polysiloxane siamine constitutes from about 28 to about 32 mole percent of the total diamines present.

3. The semiconductor element of claim 1 wherein the polysiloxanediamine constitutes 30 mole percent of the total diamines present.

4. The semiconductor element of claim 1 wherein the material of the layer of the conformal protective coat-

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ing material contains at least one electrically insulating material admixed therein.

5. The semiconductor element of claim 4 in which the electrically insulating material is a material selected from the group consisting of aluminum oxide, silicon oxide, glass fibers, boron nitride, quartz, mica, magnesium oxide and activated polytetrafluorethylene.

6. The semiconductor element of claim 1 including a finely divided electrically insulating material uniformly distributed throughout the layer of conformal protective coating material.

7. The semiconductor element of claim 6 in which the electrically insulating material is a material selected from the group consisting of aluminum oxide, silicon oxide, glass fibers, boron nitride, quartz, mica, magnesium oxide, and reactivated polytetrafluorethylene.

8. The semiconductor element of claim 1 including a layer of an electrically insulating material selected from the group consisting of aluminum nitride, silicon oxide and silicon nitride deposited on the exposed end portion of the at least one P-N junction beneath the layer of conformal protective coating material.

9. The semiconductor element of claim 1 including a layer of an electrically insulating material selected from the group consisting of aluminum nitride, silicon oxide and silicon nitride deposited on the exposed end portion of the at least one P-N junction and beneath the layer of protective coating material.

\* \* \* \* \*



US006700209B1

(12) **United States Patent**  
**Raiser et al.**

(10) **Patent No.:** **US 6,700,209 B1**  
(45) **Date of Patent:** **\*Mar. 2, 2004**

(54) **PARTIAL UNDERFILL FOR FLIP-CHIP  
ELECTRONIC PACKAGES**

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(\*) **Notice:** This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 332 days.

(21) **Appl. No.:** **09/474,746**

(22) **Filed:** **Dec. 29, 1999**

(51) **Int. Cl.<sup>7</sup>** ..... **H01L 23/29; H01L 23/28;**  
**H01L 23/48; H01L 23/52**

(52) **U.S. Cl.** ..... **257/790; 257/787; 257/782;**  
**257/778; 257/737; 257/738; 257/780**

(58) **Field of Search** ..... **257/778, 789,**  
**257/795, 787, 779, 780, 738**

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*Primary Examiner*—Tom Thomas

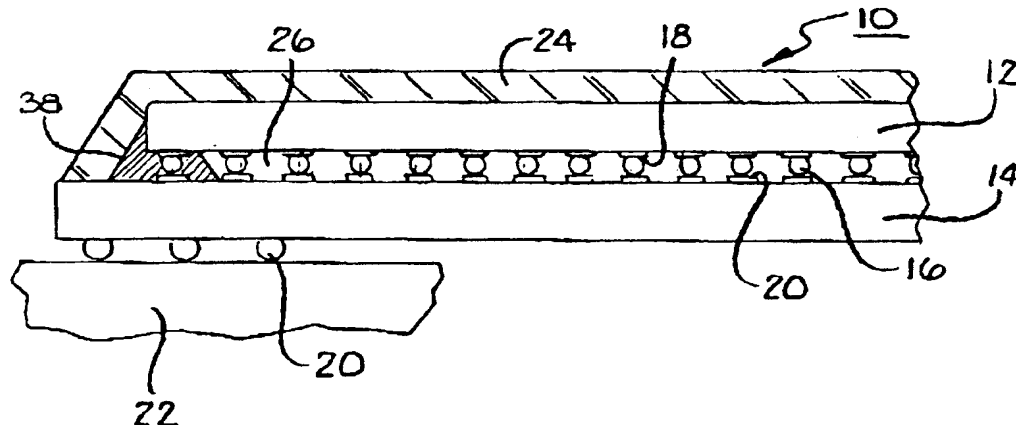
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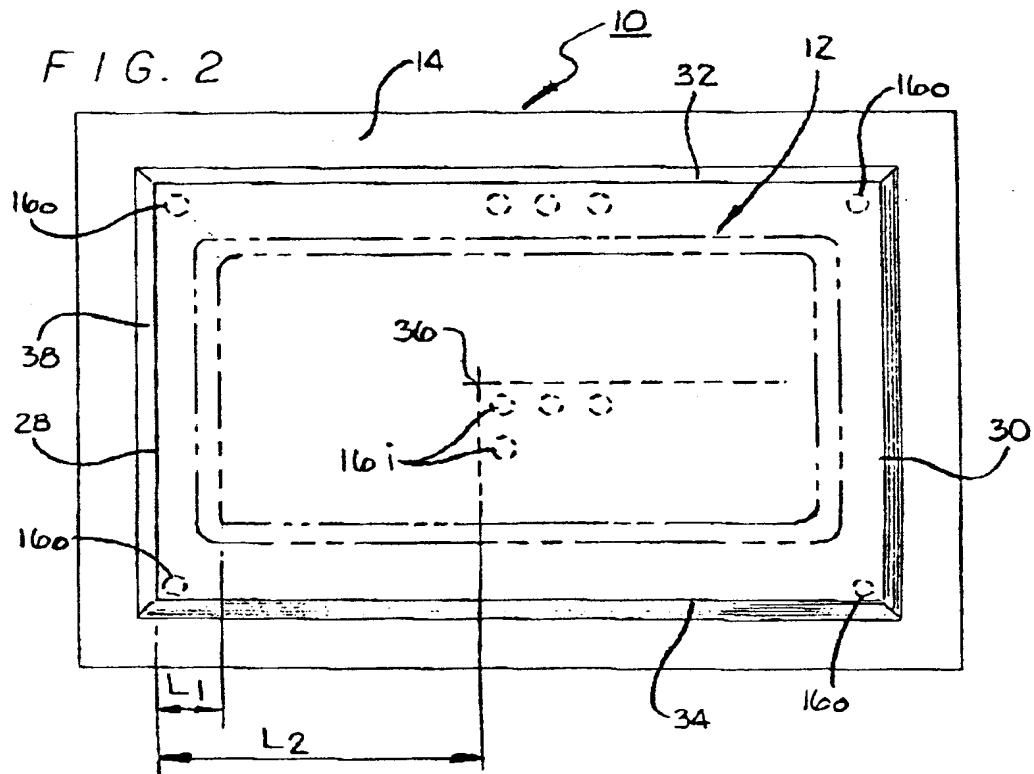
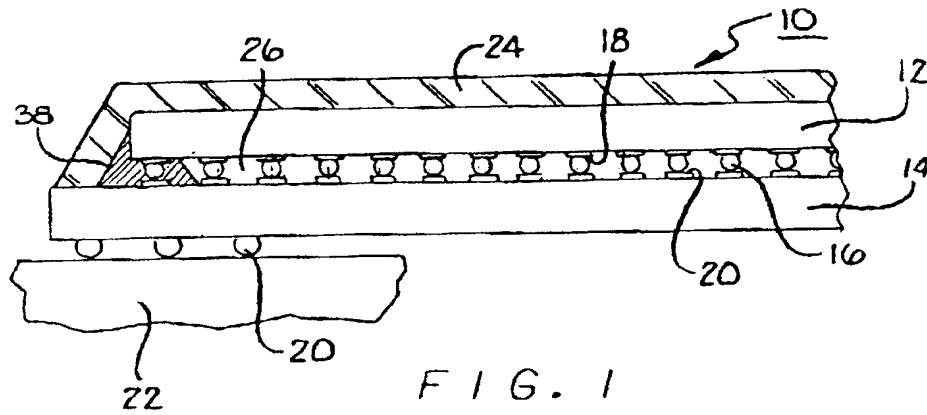
(74) *Attorney, Agent, or Firm*—Blakely, Sokoloff, Taylor & Zafman LLP

(57) **ABSTRACT**

An integrated circuit package that contains an underfill material between an integrated circuit and a substrate. The integrated circuit may be mounted to the substrate with solder bumps in a C4 process. The underfill material may extend from an edge of the integrated circuit a length that is no less than approximately 25% of the length between the integrated circuit edge and the integrated circuit center. It has been discovered that a length greater than approximately 25% does not provide a significant reduction in the strain of the solder bumps.

**12 Claims, 3 Drawing Sheets**





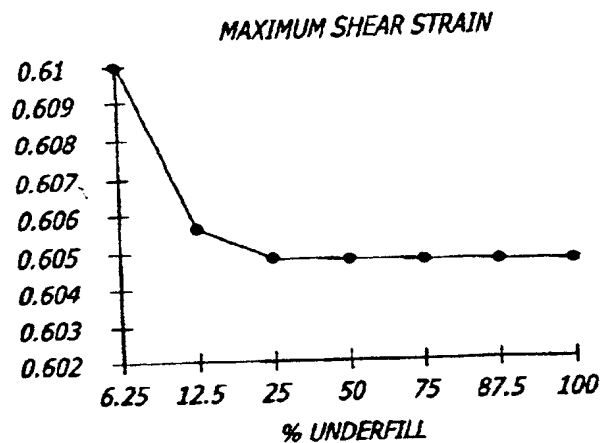


FIG. 3a

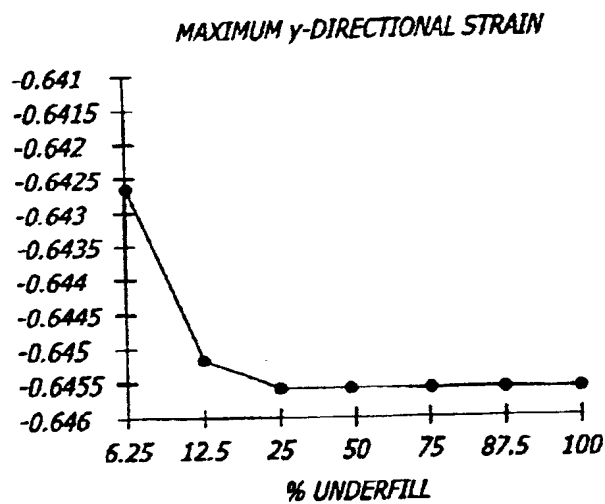


FIG. 3b

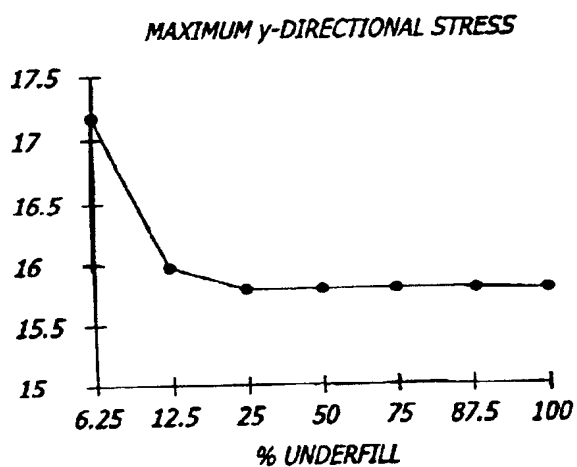


FIG. 3c

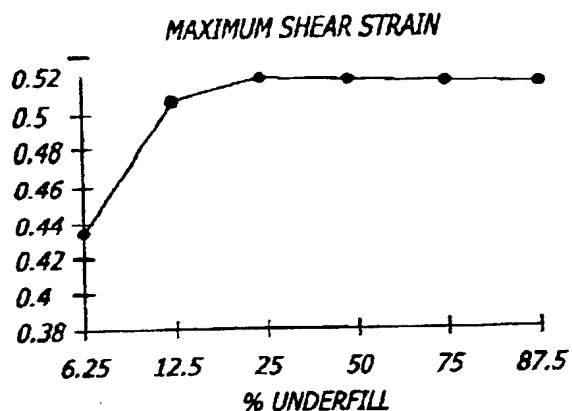


FIG. 4a

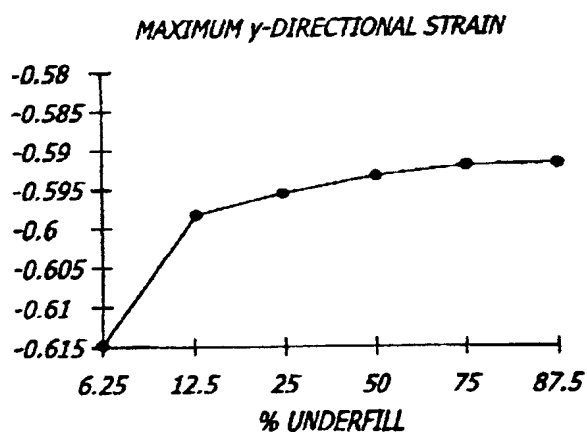


FIG. 4b

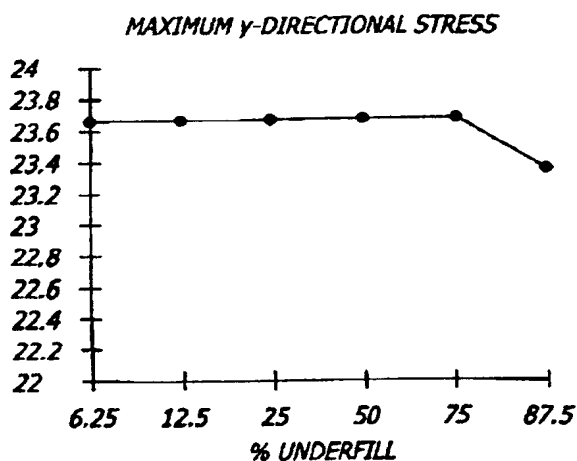


FIG. 4c

# PARTIAL UNDERFILL FOR FLIP-CHIP ELECTRONIC PACKAGES

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to an underfill for a C4 integrated circuit package.

### 2. Background Information

Integrated circuits are typically assembled into packages that are mounted to a printed circuit board. The package may include a substrate that has solder balls or other types of contacts that are attached to the circuit board. An integrated circuit is mounted to the substrate. The substrate typically has routing traces, vias, etc. that electrically connect the integrated circuit to the solder balls.

The integrated circuit may be connected to corresponding surface pads of the substrate with solder bumps in a process commonly referred to as controlled collapsed chip connection (C4). The substrate coefficient of thermal expansion is different than the coefficient of thermal expansion for the integrated circuit. When the package is thermally cycled the difference in thermal expansion may create a mechanical strain in the solder bumps. It has been found that the strain may create cracks and corresponding electrical opens in the solder bumps, particularly after a number of thermal cycles.

Most C4 packages contain an underfill material that is formed between the integrated circuit and the substrate. The underfill material structurally reinforces the solder bumps and improves the life and reliability of the package. The underfill material is typically dispensed onto the substrate in a liquid or semi-liquid form. The liquid underfill then flows between the integrated circuit and the substrate under a capillary action. The liquid underfill is eventually cured into a solid state.

The underfill process completely fills the space between the integrated circuit and the substrate to structurally reinforce all of the solder bumps. A number of techniques have been developed to insure that the underfill material surrounds all of the solder bumps. It is desirable to fill the space between the integrated circuit and the substrate to insure that gases are not trapped within the substrate/integrated circuit interface. The gases may escape during subsequent process steps, particularly if the package is heated and re-flowed onto a motherboard. The release of gases may cause a delamination of the package.

## SUMMARY OF THE INVENTION

One embodiment of the present invention is an integrated circuit package that contains an underfill material. The underfill material may extend from an outer edge of the integrated circuit towards the center of the integrated circuit a length  $L_1$  that is no less than approximately 25% of a length  $L_2$  between the edges and a center of the integrated circuit.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a side sectional view of an embodiment of an integrated circuit package of the present invention;

FIG. 2 is a top sectional view of the integrated circuit package;

FIG. 3a is a graph showing a shear strain of an outermost solder bump versus an underfill percentage;

FIG. 3b is a graph showing a y-axis directional strain of the outermost solder bump;

FIG. 3c is a graph showing a y-axis directional stress of the outermost solder bump;

FIG. 4a is a graph showing a shear strain of an outermost unsupported solder bump versus an underfill percentage;

FIG. 4b is a graph showing a y-axis directional strain of the unsupported outermost solder bump;

FIG. 4c is a graph showing a y-axis directional stress of the unsupported outermost solder bump.

## DETAILED DESCRIPTION

Referring to the drawings more particularly by reference numbers, FIGS. 1 and 2 show an embodiment of an integrated circuit package 10 of the present invention. The package 10 may include an integrated circuit 12 that is mounted to a package substrate 14. The package 10 may further include a plurality of solder bumps 16 that are connected to die pads 18 of the integrated circuit 12 and corresponding conductive surface pads 20 of the substrate 14. The solder bumps 16 are typically assembled with a process commonly referred to as controlled collapsed chip connection (C4).

The package 10 may include a plurality of solder balls 20 that are attached to the substrate 14. The solder balls 20 may be re-flowed to attach the package 10 to a substrate 22. The package substrate 14 may have routing traces, vias, etc. (not shown) that electrically connect the solder bumps 16 to the solder balls 20. The integrated circuit 12 may be enclosed by an encapsulant or heat spreader 24.

The package 10 may include an underfill material 26 that is located at the interface of the integrated circuit 12 and the substrate 14. The underfill 26 may be an epoxy material that structurally reinforces the solder bumps 16, particularly when the package 10 is thermally cycled.

The integrated circuit 12 may have a first edge 28, a second edge 30, a third edge 32 and a fourth edge 34. The underfill material 26 may extend from the edges of the integrated circuit to a center point 36 of the integrated circuit 12. The underfill material 26 may be assembled into the package 10 so that a fillet 38 is formed along the entire perimeter of the integrated circuit 12. By way of example, the fillet 38 may extend from the substrate 14 to a point approximately one-half the thickness of the integrated circuit 12.

It has been found that the underfill material 26 does not have to completely fill the space between the integrated circuit 12 and the substrate 14 to adequately support the solder bumps 16. FIGS. 3a-c show the shear strain, y-axis directional strain and y-axis directional stress of the solder bumps 16 at the outermost portion of the package versus a percentage of underfill material 26. The outermost solder bumps are identified as 16a in FIG. 2. The percentage of underfill material is defined as the length  $L_1$  of the underfill 26 from an edge of the integrated circuit 12 to the non-underfilled area, divided by the length  $L_2$  from the edge 28 to the center point 36 of the integrated circuit 12. The graphs are outputs from a finite element program that calculates stress and strains in response to an increase or decrease in temperature. The program was run with the following parameters:

TABLE 1

| Material          | Young's Modulus (GPa) | Poisson's Ratio ( $\nu$ ) | Coeff. of Thermal Exp. (ppm/°C) | Dimensions                 |
|-------------------|-----------------------|---------------------------|---------------------------------|----------------------------|
| Silicon Die (12)  | 129.9                 | 0.279                     | 3.3                             | 0.800" wide by 0.027" high |
| BT Substrate (14) | 23.5                  | 0.33                      | (see text)                      | 0.996" wide by 0.040" high |

TABLE 1-continued

| Material                 | Young's Modulus (GPa) | Poisson's Ratio ( $\nu$ ) | Coeff. of Thermal Exp. ( $\text{ppm}/^\circ\text{C}$ ) | Dimensions   |
|--------------------------|-----------------------|---------------------------|--|--|
| Dexter 4561 (26)         | 6.89                  | 0.30                      | 26   | Fillet from substrate to half the die thickness. Filled 0.003" - high space between substrate and die and between individual solder balls. |
| 97/3 (Pb/Sn) Solder (16) | 23.5                  | 0.35                      | 26   | Circular with 0.005" diameter cut top and bottom by the die and substrate.   |

The temperature was varied between 23 and 150 degrees centigrade.

As shown in FIGS. 3a-c, the strain and corresponding stress for the outermost solder bumps is not appreciably reduced by increasing the percentage of underfill beyond approximately 25%. It has therefore been discovered that an underfill no less than approximately 25% is required to adequately support the solder bumps 16. At another design criteria, the underfill material may have a minimum coverage of at least two times of adjacent die pads 18.

FIGS. 4a-c show the shear strain, y-axis directional strain and y-axis directional stress for the outermost solder bumps that are not surrounded by underfill material 26. One of these solder bumps is identified as 16i in FIG. 2. It being understood that the outermost solder bumps 16o and the outermost unsupported solder bumps 16i are the bumps that may have the highest strains and stresses. FIGS. 4a-c also show no appreciable decrease in strain and stress for an underfill percentage greater than approximately 25%. It is believed that the fillet 38 along each edge of the integrated circuit 12 provides enough structural integrity for the solder bumps 16. It has been discovered that the underfill material 26 does not have to completely fill the space between the circuit 12 and the substrate 14.

The package 10 can be assembled by initially mounting the integrated circuit 12 to the substrate 14 with a C4 process. Underfill material 26 may then be dispensed along each edge of the integrated circuit 12. The underfill material 26 may be dispensed in a liquid, or semi-liquid form so that the underfill 26 flows between the integrated circuit 12 and the substrate 14 under a capillary action. The volume of underfill material applied may be such that the underfill percentage is not less than approximately 25%. The underfill 26 is cured to a solid state. The solder balls 20 may be attached to the substrate 14 and the integrated circuit 12 may be enclosed with the encapsulant or heat spreader 24 to complete the package 10.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art.

What is claimed is:

1. An integrated circuit package comprising:

a package substrate;

an integrated circuit mounted to said package substrate, wherein said integrated circuit includes an outer boundary;

an underfill material having an underfill material inner boundary situated between said integrated circuit and said package substrate and substantially spaced apart from a center region of said integrated circuit to define a non-filled space between said integrated circuit and said package substrate, and an underfill material outer boundary extending beyond said integrated circuit outer boundary, wherein said underfill material occupies approximately 25% of the space between the integrated circuit and the package substrate, and said non-filled space occupies approximately 75% of the space between the integrated circuit and the package substrate; and,

an encapsulant disposed over said integrated circuit and having an encapsulant material and an encapsulant outer boundary that extends beyond said integrated circuit outer boundary wherein said encapsulant material is different from said underfill material.

2. The integrated circuit package of claim 1 wherein said underfill material outer boundary extends from said package substrate to approximately one-half of a thickness of said integrated circuit.

3. The integrated circuit package of claim 1 wherein said integrated circuit includes a plurality of die pads, and said underfill material inner boundary extends at least two times a distance between adjacent die pads.

4. The integrated circuit package of claim 1 wherein said underfill material outer boundary extends from said substrate package a distance of one-half of a perimeter of said integrated circuit.

5. An integrated circuit package comprising:

a package substrate;

an integrated circuit mounted to said package substrate, wherein said integrated circuit includes an outer boundary;

an underfill material having an underfill material inner boundary situated between said integrated circuit and said package substrate and substantially spaced apart from a center region of said integrated circuit to define a non-filled space between said integrated circuit and said package substrate, and an underfill material outer boundary extending beyond said integrated circuit outer boundary and forming a fillet at a perimeter of said integrated circuit, wherein said underfill material occupies approximately 25% of the space between the integrated circuit and the package substrate, and said non-filled space occupies approximately 75% of the space between the integrated circuit and the package substrate; and,

an encapsulant disposed over said integrated circuit and having encapsulant material and an encapsulant outer boundary that extend beyond said integrated circuit outer boundary wherein said encapsulant material is different from said underfill material.

6. The integrated circuit package of claim 5 wherein said underfill material outer boundary extends from said package substrate to approximately one-half of a thickness of said integrated circuit.

7. The integrated circuit package of claim 5 wherein said integrated circuit includes a plurality of die pads, and said underfill material inner boundary extends at least two times a distance between adjacent die pads.

8. The integrated circuit package of claim 5 wherein said underfill material outer boundary extends from said substrate package a distance of one-half of a perimeter of said integrated circuit.

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9. An integrated circuit package comprising:  
 a package substrate;  
 an integrated circuit mounted to said package substrate,  
 wherein said integrated circuit includes an outer bound-  
 ary;  
 an underfill material having an underfill material inner  
 boundary situated between said integrated circuit and  
 said package substrate and substantially spaced apart  
 from a center region of said integrated circuit to define  
 a non-filled space between said integrated circuit and  
 said package substrate, and an underfill material outer  
 boundary forming a fillet at a perimeter of said inte-  
 grated circuit, wherein said underfill material occupies  
 approximately 25% of the space between the integrated  
 circuit and the package substrate, and said non-filled  
 space occupies approximately 75% of the space  
 between the integrated circuit and the package sub-  
 strate; and,

6

an encapsulant disposed over said integrated circuit and  
 having an encapsulant material and an encapsulant  
 outer boundary that extend beyond said integrated  
 circuit outer boundary wherein said encapsulant mate-  
 rial is different from said underfill material.

10. The integrated circuit package of claim 9 wherein said  
 underfill material outer boundary extends from said package  
 substrate to approximately one-half of a thickness of said  
 integrated circuit.

11. The integrated circuit package of claim 9 wherein said  
 integrated circuit includes a plurality of die pads, and said  
 underfill material inner boundary extends at least two times  
 a distance between adjacent die pads.

12. The integrated circuit package of claim 9 wherein said  
 underfill material outer boundary extends from said sub-  
 strate package a distance of one-half of a perimeter of said  
 integrated circuit.

\* \* \* \* \*





US005973930A

**United States Patent** [19]

Ikeda et al.

[11] **Patent Number:** 5,973,930[45] **Date of Patent:** Oct. 26, 1999[54] **MOUNTING STRUCTURE FOR ONE OR MORE SEMICONDUCTOR DEVICES**[75] Inventors: **Hironobu Ikeda; Yukio Yamaguti**,  
both of Tokyo, Japan[73] Assignee: **NEC Corporation**, Tokyo, Japan[21] Appl. No.: **09/111,871**[22] Filed: **Jul. 8, 1998**[30] **Foreign Application Priority Data**

Aug. 6, 1997 [JP] Japan ..... 9-212065

[51] Int. Cl.<sup>6</sup> ..... **H05K 1/11; H05K 7/06;**  
H01L 23/488[52] U.S. Cl. .... **361/768; 361/803; 257/723;**  
257/778[58] **Field of Search** ..... 361/743, 767,  
361/768, 783, 784, 803; 257/686, 723,  
777, 778[56] **References Cited****U.S. PATENT DOCUMENTS**

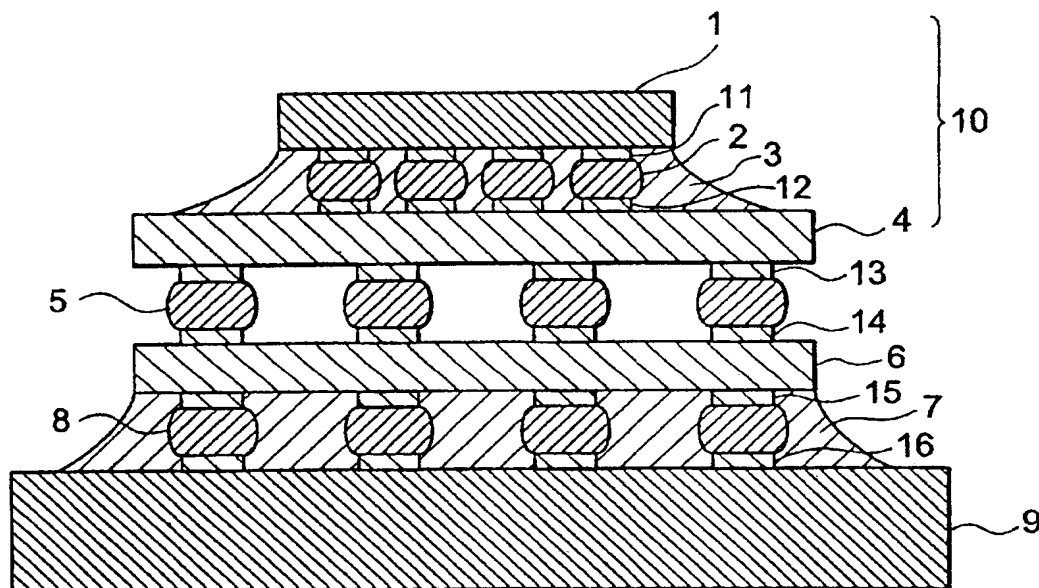
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*Primary Examiner*—Leo P. Picard*Assistant Examiner*—John B. Vigushin*Attorney, Agent, or Firm*—Sughrue, Mion, Zinn, Macpeak  
& Seas, PLLC[57] **ABSTRACT**

A mounting structure wherein, in a semiconductor package mounting position on a wiring board, a package bearing substrate whose external size is substantially equal to or larger than that of the semiconductor package and which has on its upper surface pads for connection to a semiconductor package and on its lower surface pads for connection to the wiring board is arranged, the pads on the wiring board and those on the lower surface of the package bearing substrate are connected by soldering, and the soldered junction is filled and fixed with an under-fill.

**9 Claims, 7 Drawing Sheets**

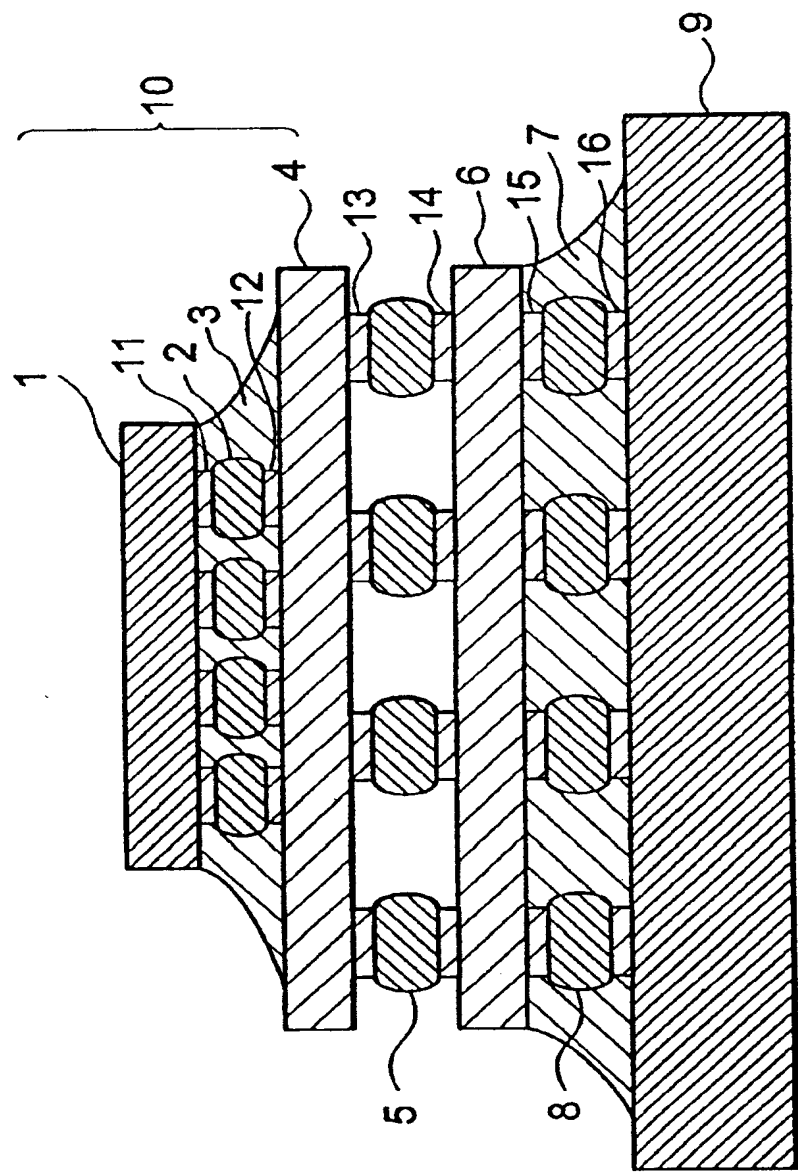


FIG. 1

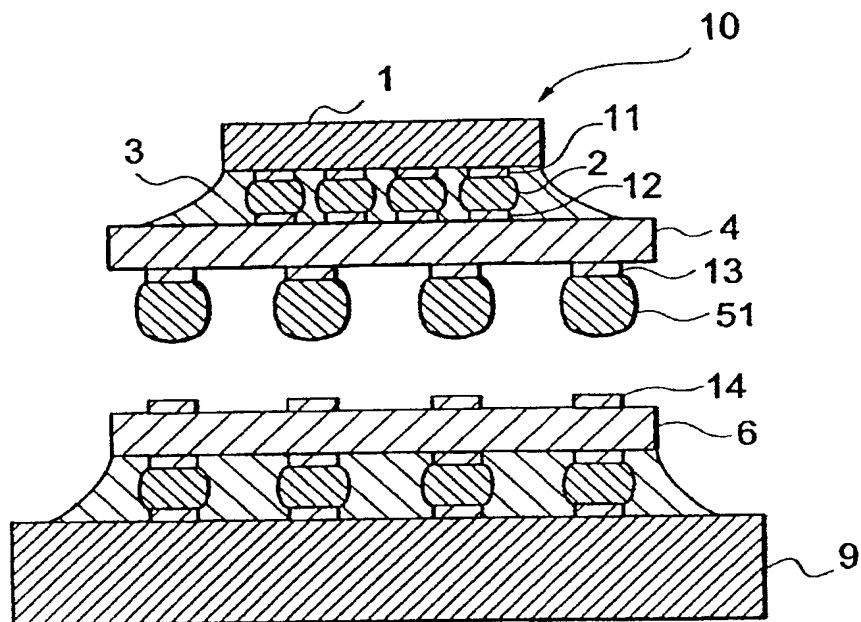


FIG. 2 A

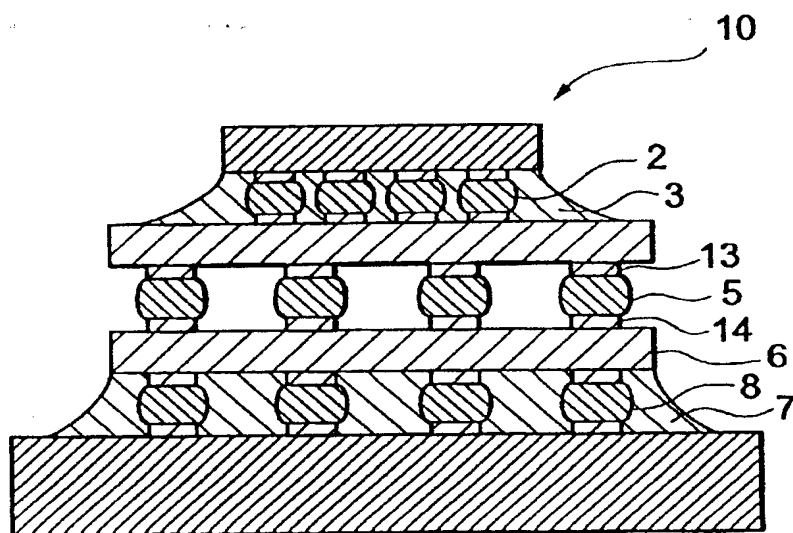


FIG. 2 B

FIG. 3 A

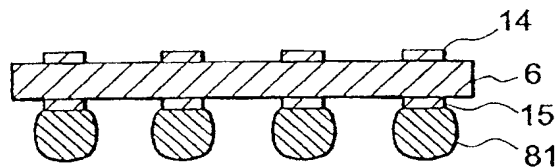


FIG. 3 B

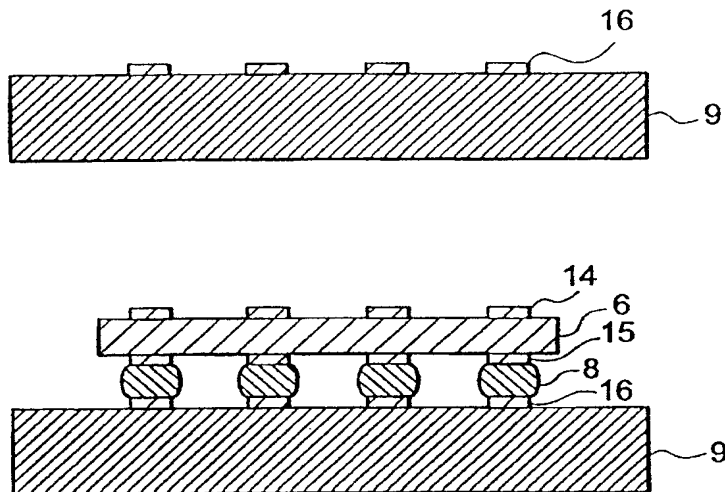
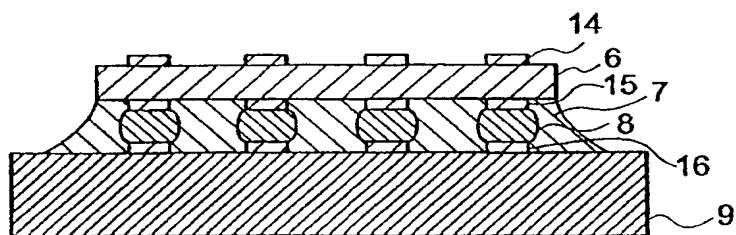


FIG. 3 C



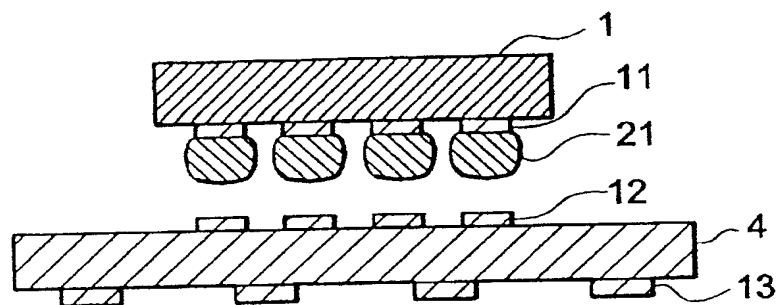


FIG. 4 A

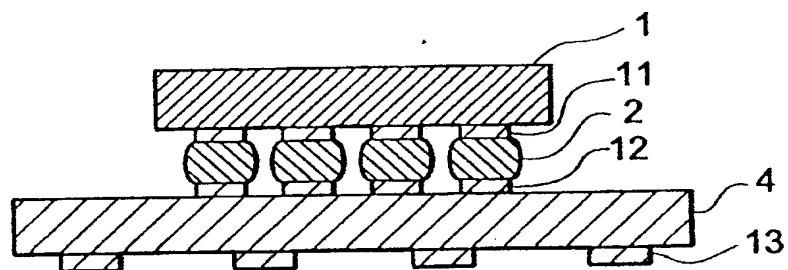


FIG. 4 B

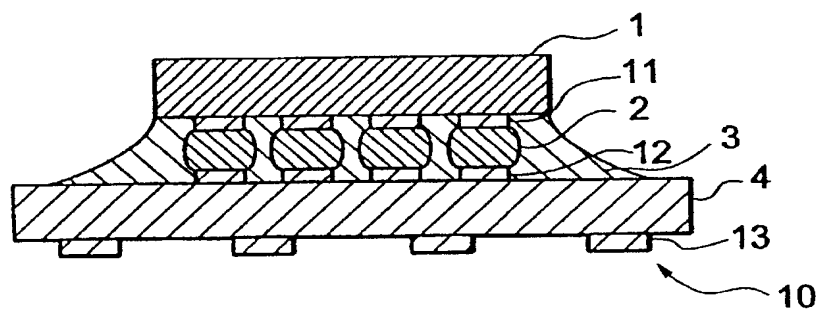


FIG. 4 C

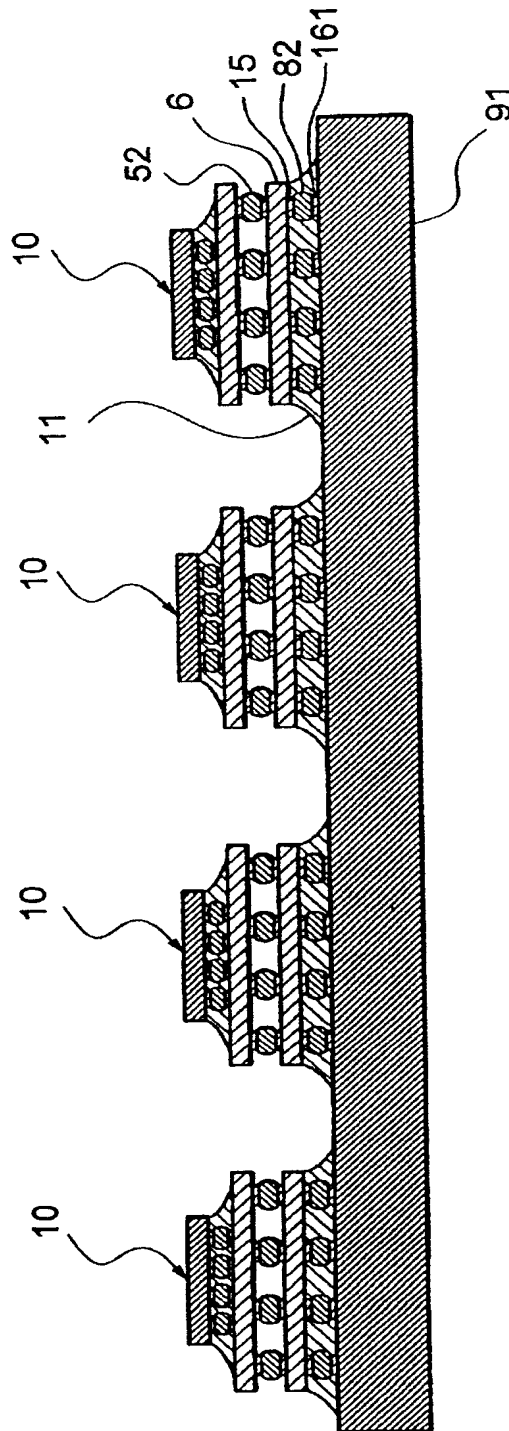


FIG. 5

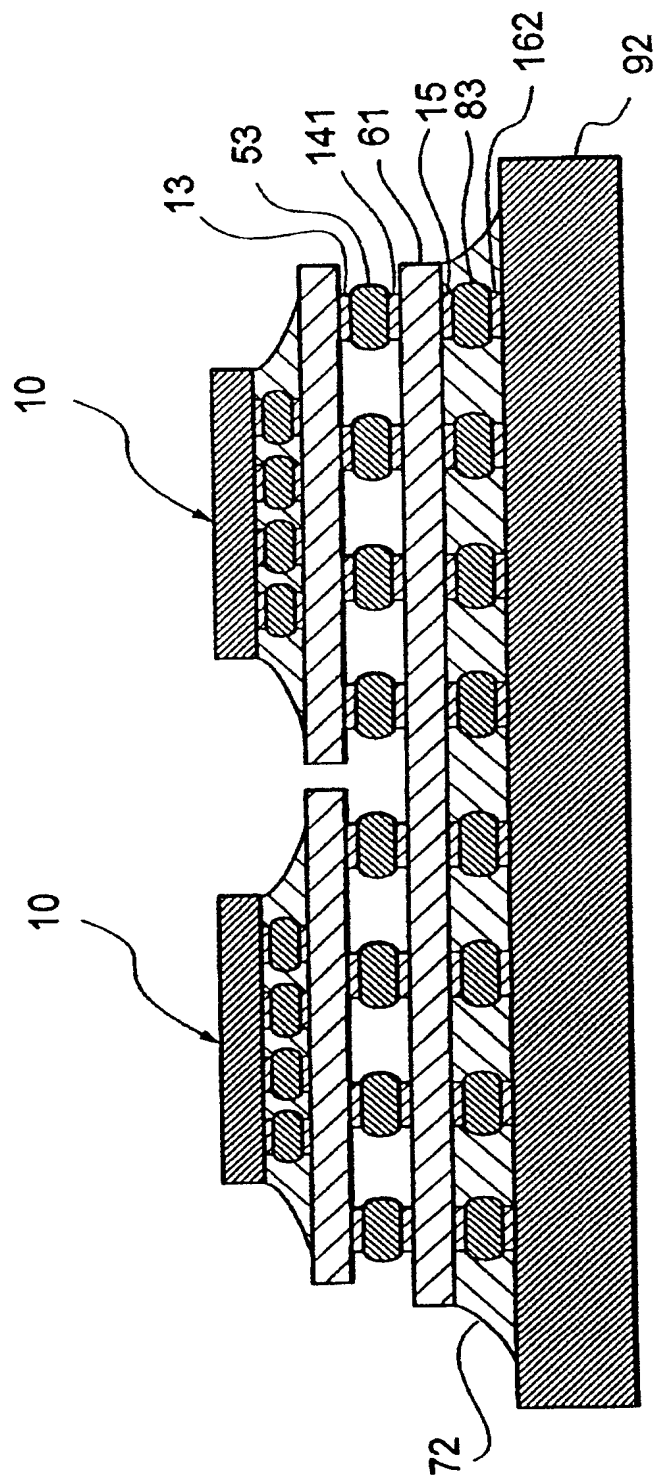


FIG. 6

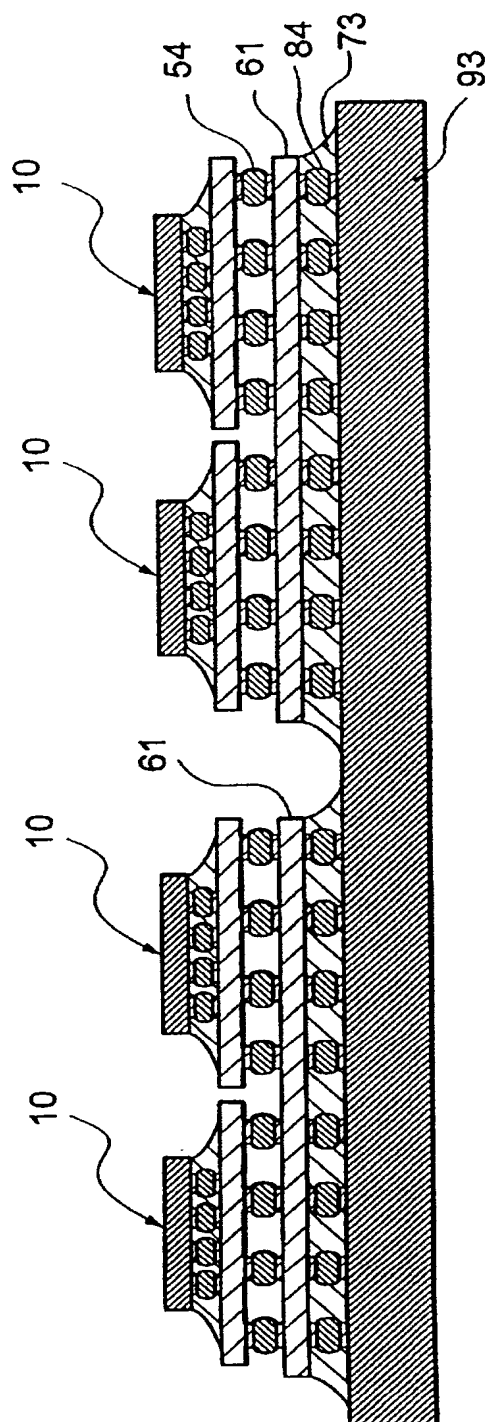


FIG. 7



# MOUNTING STRUCTURE FOR ONE OR MORE SEMICONDUCTOR DEVICES

## BACKGROUND OF THE INVENTION

The present invention relates to a mounting structure for one or more semiconductor devices, and more particularly to a mounting structure for one or more semiconductor devices allowing packaging in substantially the same size as the semiconductor device or devices and multi-pin mounting in high density.

A conventional semiconductor device mounting structure is disclosed in Japanese Patent Application Laid-open No. Hei 4-154136.

The mounting structure for semiconductor devices described in the Japanese Patent Application has a film carrier interposed between a bare chip and a substrate. The basic material of the film carrier is either a ceramic, such as alumina or aluminum nitride, or an organic material, such as polyimide or Teflon. On the upper surface of the film carrier are arranged pads for connection to the electrodes of flip chips, and on its lower surface are pads for connection to the electrodes of the substrate. Junctions between the flip chips and the film carrier may be Au (gold) to Au junctions, Au to Sn (tin) junctions or the like, and the film carrier and the substrate are soldered to each other.

Generally, where a semiconductor package mounted with a bare chip is to be mounted on a wiring board, it is necessary to match the thermal expansion coefficient of the semiconductor package itself and that of the wiring board, or where the difference in thermal expansion coefficient between the two is significant, it is necessary to disperse the stress in the junction and improve the reliability of connection by sealing in an under-filling material or the like.

However, the prior art referred to above takes no account of the thermal expansion coefficients of the bare chip and the film carrier. In order to secure the connection reliability of the junction between the bare chip and the film carrier, the basic material of the film carrier should preferably be aluminum nitride, whose thermal expansion coefficient is close to that of silicon (Si) chips, but the use of this material would give rise to the problem of a difference in thermal expansion coefficient between aluminum nitride and the wiring board and, if the film carrier is mounted on a printed circuit board having a high thermal expansion coefficient, a problem would arise as to the reliability of connection between the film substrate and the printed circuit board.

Where a bare chip is to be directly mounted on a printed circuit board, it is also common to seal in an under-filling material between the bare chip and the printed circuit board to ensure the connection reliability of the junction, but in the event of serious enough trouble with the bare chip to necessitate its replacement, the fixation with the under-filling material makes it prohibitively difficult to replace the bare chip.

An object of the present invention is to provide a mounting structure for one or more semiconductor devices, of which the external contour of the package is substantially as large as that of the integrated circuit chip, and which permits multi-pin connection and high-density packaging.

Another object of the invention is to provide a mounting structure for one or more semiconductor devices using a printed circuit board, which is inexpensive as a substrate on which to mount a semiconductor device and compatible with a large size.

Still another object of the invention is to provide a mounting structure permitting ready replacement of a defective or broken-down semiconductor device.

## SUMMARY OF THE INVENTION

A mounting structure for one or more semiconductor devices according to the invention uses a wiring board for mounting a semiconductor package, which includes a semiconductor device, wherein a package bearing substrate whose external size is substantially equal to or larger than that of said semiconductor package and which has electrodes for connection to said semiconductor package on its upper surface and electrodes for connection to said wiring board on its lower surface is arranged in the position of mounting said semiconductor package on said wiring board; the electrodes of said wiring board and those on the lower surface of said package bearing substrate are connected by soldering, and the soldered connection part is filled with an under-filling material to fix said wiring board and said package bearing substrate together.

Another mounting structure for one or more semiconductor devices according to the invention is provided with a plurality of package bearing substrates arranged on said wiring board.

Still another mounting structure for one or more semiconductor devices according to the invention is provided with one of said semiconductor package is connected onto one package bearing substrate on said wiring board by soldering.

Yet another mounting structure for one or more semiconductor devices according to the invention is provided with a plurality of package bearing substrates arranged on said wiring board, and one of said semiconductor packages is connected to one package bearing substrate by soldering.

Another mounting structure for one or more semiconductor devices according to the invention is provided with a plurality of said semiconductor packages connected with solder bumps to one package bearing substrate arranged on said wiring board.

Still another mounting structure for one or more semiconductor devices according to the invention is provided with a plurality of package bearing substrates arranged on said wiring board, wherein a plurality of said semiconductor packages are connected with solder bumps to one package bearing substrate.

In another mounting structure for one or more semiconductor devices according to the invention, the thermal expansion coefficient of the package substrate bearing substrate arranged on said wiring board is substantially equal to that of said semiconductor package.

In still another mounting structure for one or more semiconductor devices according to the invention, the difference between the thermal expansion coefficient of the package substrate bearing substrate arranged on said wiring board and that of said semiconductor package is not more than 50% of the thermal expansion coefficient of said semiconductor package.

In yet another mounting structure for one or more semiconductor devices according to the invention, the melting point of the solder connecting said wiring board and the package bearing substrate arranged on said wiring board is the same as that of the solder connecting said package bearing substrate and said semiconductor package.

In another mounting structure for one or more semiconductor devices according to the invention, the melting point of the solder connecting said wiring board and the package bearing substrate arranged on said wiring board is higher than that of the solder connecting said package bearing substrate and said semiconductor package.

## BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 shows a cross-sectional view of a first preferred embodiment of the invention;

FIGS. 2A and 2B show cross-sectional views illustrating aspects of a manufacturing method for the first preferred embodiment of the invention;

FIGS. 3A to 3C shows cross-sectional views illustrating other aspects of the manufacturing method for the first embodiment of the invention;

FIGS. 4A to 4C are cross-sectional views illustrating further aspects of the manufacturing method for the first embodiment of the invention;

FIG. 5 shows a cross-sectional view of a second preferred embodiment of the invention;

FIG. 6 shows a cross-sectional view of a third preferred embodiment of the invention; and

FIG. 7 shows a cross-sectional view of a fourth preferred embodiment of the invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Description will next be made in detail on a mounting structure for one or more semiconductor devices of the present invention, with reference to the accompanying drawings.

Referring to FIG. 1, a first embodiment of the mounting structure of the invention comprises a semiconductor package 10 including a semiconductor device 1; a package bearing substrate 6 for mounting the semiconductor package 10; solder pieces 5 for electrically and mechanically connecting the semiconductor package 10 and the package bearing substrate 6; a wiring board 9 for mounting the package bearing substrate 6; solder pieces 8 for electrically and mechanically connecting the package bearing substrate 6 and the wiring board 9; and an under-fill 7 filling the gap between the package bearing substrate 6 and the wiring board 9.

If the external dimensions of the package bearing substrate 6 are 30 mm×30 mm and the spacing between adjoining pads 15 on the lower surface of the package bearing substrate 6 is 1 mm, about 900 pads 15 can be arranged in a grid pattern. Pads 16 arranged on the upper surface of the wiring board are disposed in positions matching the pads 15 on the lower surface of the package bearing substrate 6, and the pads 16 on the upper surface of the wiring board 9 and the pads 15 on the lower surface of the package bearing substrate 6 are connected to each other by the solder pieces 8. Where a common printed circuit board is used as wiring board 9 and a ceramic material is used for the package bearing substrate 6, stresses due to a difference in thermal expansion coefficient arise in the soldered parts and the padded parts. While the thermal expansion coefficient of the printed circuit board is 20 to 30 ppm, that of a ceramic material, for instance alumina, is about 7 ppm, resulting in a wide difference in thermal expansion coefficient, that of the printed circuit board being three to four times as high as that of alumina. If the temperature varies, the two will expand or contract differently, and this difference will give rise to concentrated stresses in the soldered parts and the padded parts. These stresses would invite cracks in solder or cause pads to come off, possibly resulting in electrical

openness. To avoid this problem, the gap between the package bearing substrate 6 and the wiring board 9 is filled with the under-fill 7 of, for instance epoxy resin, to fix them firmly together. The under-fill 7 serves to disperse the stresses caused by the difference in thermal expansion, making it possible to prevent the soldered parts from cracking and the pads from coming off.

FIG. 2A is a cross-sectional view illustrating the semiconductor package 10 and the package bearing substrate 6 fitted on the wiring board 9. As shown in FIG. 2A, the semiconductor package 10 mounted on the package bearing substrate 6 is a ball grid array (BGA) type package having solder bumps 51 as external terminals. On the circuit plane of the lower surface of the semiconductor device 1 are arranged pads 11 in either a grid pattern or near the periphery. The semiconductor device 1 is mounted on a carrier substrate 4 having on its upper surface pads 12 arranged in the same manner as the pads 11. The pads 11 of the semiconductor device 1 and the pads 12 on the upper surface of the carrier substrate 4 are connected with solder pieces 2, and the gap between the semiconductor device 1 and the carrier substrate 4 is filled with an under-fill 3. If the external dimensions of the semiconductor device 1 are 15 mm×15 mm and the spacing between adjoining pads 11 of the semiconductor device 1 is 0.5 mm, about 900 pads 11 can be arranged in a grid pattern. The pads 12 on the upper surface of the carrier substrate 4 are arranged in the same manner as the pads 11 of the semiconductor device 1 are. The external dimensions of the carrier substrate are 30 mm×30 mm, and 900 pads 13 are arranged on the lower surface of the carrier substrate 4 at 1 mm intervals in a grid pattern as the pads 14 on the upper surface of said package bearing substrate 6 are. The pads 12 on the upper surface and the pads 13 on the lower surface, both of the carrier substrate 4, are connected to each other as desired by wiring in inner and outer layers of the carrier substrate 4. As the extremely narrow 0.5 mm spacing of the pads 12 on the upper surface of the carrier substrate 4 makes it difficult to manufacture this substrate out of a usual through-hole type printed circuit board, it is desirable to use a ceramic material, such as alumina, for the carrier substrate 4. The semiconductor device 1 is made of silicon, whose thermal expansion coefficient is about 3 ppm. On the other hand, if the carrier substrate 4 is made of alumina, its thermal expansion coefficient is about 7 ppm. As stated above, this difference in thermal expansion coefficient between the semiconductor device 1 and the carrier substrate 4 will give rise to concentrated stresses in the soldered parts and the padded parts connecting them, and might invite cracks in solder or cause pads to come off. To avoid this problem, the gap between the semiconductor device 1 and the carrier substrate 4 is filled with the under-fill 3 to disperse the stresses caused by the difference in thermal expansion, making it possible to secure the connection reliability of the junction. The under-fill 3, which may consist of epoxy resin or the like, also serves to protect the circuit surface of the semiconductor device 1.

FIG. 2B is a cross-sectional view illustrating a configuration in which the semiconductor package 10 is arranged on the wiring board 9. The external shape of the carrier substrate 4 of the semiconductor package 10 and that of the package bearing substrate 6 are substantially the same, and the arrangement of the pads 13 on the lower surface of the carrier substrate 4 of the semiconductor package 10 and that of the pads 14 on the upper surface of said package bearing substrate 6 are the same, the pads 13 and 14 being electrically and mechanically connected to each other by the solder pieces 5. Even if the carrier substrate 4 and the package

bearing substrate 6 differ in external shape, there will be no problem if the pads 13 and the pads 14 are arranged in the same manner. The material of the carrier substrate 4 should be the same as that of the package bearing substrate 6. For instance, if alumina is used for the carrier substrate 4, the package bearing substrate 6 should also be made of alumina. By using the same material for the carrier substrate 4 and the package bearing substrate 6, the difference in thermal expansion coefficient between the carrier substrate 4 and the package bearing substrate 6 can be reduced to zero, and concentrated stresses invited by any temperature variation in the solder pieces 5 and the pads 13 and 14 can be brought infinitely close to zero. Accordingly, connection reliability can be secured without having to fill the gap between the carrier substrate 4 and the package bearing substrate 6 with an under-filling material as stated above.

Although it was stated that the same material should be used for the carrier substrate 4 and the package bearing substrate 6, if the difference in thermal expansion coefficient between the carrier substrate 4 and the package bearing substrate 6 is not more than 50% of the thermal expansion coefficient of the carrier substrate 4, there will be no great enough stresses working on the solder pieces 5 and the pads 13 and 14 to create a problem. Examples of materials to be used include glass ceramic, whose thermal expansion coefficient is about 5 ppm, for the carrier substrate 4, and alumina ceramic, about 7 ppm in thermal expansion coefficient, for the package bearing substrate 6.

In the event that the semiconductor device 1 runs into trouble, the semiconductor package 10 will have to be replaced. Whereas the replacement would require heating until the solder pieces 5, connecting the pads 13 of the carrier substrate 4 and the pads 14 of the package bearing substrate 6, are melted, the solder pieces 2 connecting the semiconductor device 1 and the carrier substrate 4, if they have the same melting point as the solder pieces 5, will also be melted then, but the semiconductor device 1 and the carrier substrate 4, as they are stuck together by the under-fill 3, will not separate from each other. Similarly, the solder pieces 8 connecting the package bearing substrate 6 and the wiring board 9, if they have the same melting point as the solder pieces 5, will also be melted then, but the wiring board 9 and the package bearing substrate 6, as they are stuck together by the under-fill 7, will not separate from each other. Therefore, the semiconductor package 10 can be readily replaced by melting the solder pieces 5. The solder for use in connecting the carrier substrate 4 and the package bearing substrate 6 may be eutectic solder consisting, for instance, of Sn and Pb in a 63/37 weight ratio, and similarly eutectic solder is used for the solder pieces 2 and 8. If a solder having a higher melting point than that for the solder pieces 5, for example one of Sn and Pb in a 10/90 weight ratio, is used for the solder pieces 2 and 8, only the solder pieces 5 connecting the carrier substrate 4 and the package bearing substrate 6 can be melted when the semiconductor package 10 is to be replaced, without melting the solder pieces 2 connecting the semiconductor device 1 and the carrier substrate 4 or the solder pieces 8 connecting the package bearing substrate 6 and the wiring board 9.

Next will be described in detail a manufacturing method for the mounting structure for semiconductor devices according to the invention with reference to accompanying drawings.

First will be described a step to fit the package bearing substrate 6 onto the wiring board 9.

Referring to FIG. 3A, solder bumps 81 are provided over the pads 15 on the lower surface of the package bearing

substrate 6. One way to provide the solder bumps 81 is to supply cream solder onto the pads 15 of the package bearing substrate 6 by screen printing, and perform heated reflowing, i.e. heating the cream solder at 210° C. if it is eutectic solder of Sn and Pb in a 63/37 weight ratio. The cream solder will then be melted to form the hemispherical solder bumps 81. Another way is to arrange solder balls, so shaped in advance, over the pads 15 and subject them to heated reflowing. Where the space between adjoining pads 15 on the package bearing substrate 6 is 1 mm, the pads 15 should desirably be spherical, measuring about 0.5 mm in diameter, and the height of the solder bumps 81 should preferably be 0.5 to 0.7 mm approximately.

Next, the pads 16 on the wiring board 9 and the solder bumps 81 on the package bearing substrate 6 are aligned to overlap each other and subjected to heated reflowing so that, as illustrated in FIG. 3B, the pads 15 of the package bearing substrate 6 and the pads 16 of the wiring board 9 are electrically and mechanically connected to each other by the solder pieces 8. The size of the pads 16 on the wiring board 9 should preferably be substantially equal to that of the pads 15 of the package bearing substrate 6. A gap of about 0.5 mm is secured between the package bearing substrate 6 and the wiring board 9 by the surface tension of the solder pieces 8.

The next step is that of filling the gap between the package bearing substrate 6 and the wiring board 9 with the under-fill 7 as shown in FIG. 3C. The under-fill 7 is injected from the periphery of the package bearing substrate 6. The under-fill 7 should consist of thermosetting epoxy resin or the like, and desirably be supplied from one side or two adjoining sides of the package bearing substrate 6 to prevent any void from occurring in the gap between the package bearing substrate 6 and the wiring board 9. The under-fill 7 is injected with a dispenser, and the injected under-fill 7 permeates the gap between the package bearing substrate 6 and the wiring board 9 by capillary action. When the gap between the package bearing substrate 6 and the wiring board 9 is completely filled with the under-fill 7, the under-fill 7 is heated to its setting temperature to be hardened.

Next will be described a step to fabricate the semiconductor package 10.

Referring to FIG. 4, the manufacturing method for the semiconductor package 10 is substantially the same as the above-described method to fit the package bearing substrate 6 to the wiring board 9. As illustrated in FIG. 4A, first, solder bumps 21 are provided in advance onto the pads 11 of the semiconductor device 1. Where the spacing between adjoining pads 11 of the semiconductor device 1 is as fine as 0.5 mm, it is difficult to apply a cream solder printing method, and accordingly it is desirable to supply solder balls so shaped in advance. The solder balls are arranged over the pads 11, and subjected to heated reflowing at, for instance, 210° C. if they are made of eutectic solder of Sn and Pb in a 63/37 weight ratio, to thereby form the solder bumps 21.

Next, the pads 12 on the upper surface of the carrier substrate 4 and the solder bumps 21 on the semiconductor device 1 are aligned to overlap each other and subjected to heated reflowing so that, as illustrated in FIG. 4B, the pads 11 of the semiconductor device 1 and the pads 12 of the carrier substrate 4 are electrically and mechanically connected to each other by the solder pieces 2. The size of the pads 11 of the semiconductor device 1 should preferably be substantially equal to that of the pads 12 of the carrier substrate 4.

The next step is that of filling the gap between the semiconductor device 1 and the carrier substrate 4 with the

under-fill 3 as shown in FIG. 4C. The under-fill 3, which consists of thermosetting epoxy resin or the like as the aforementioned under-fill 7 does, should desirably be supplied from one side or two adjoining sides of the semiconductor device 1 with a dispenser to prevent any void from occurring in the gap between the semiconductor device 1 and the carrier substrate 4. When the gap between the semiconductor device 1 and the carrier substrate 4 is completely filled with the under-fill 3, the under-fill 3 is heated to its setting temperature to be hardened.

Next will be described a step to fit the semiconductor package 10 onto the package bearing substrate 6 fitted on the wiring board 9.

Referring to FIG. 2A, solder bumps 51 are provided over the pads 13 on the lower surface of the carrier substrate 4 of the semiconductor package 10. One way to provide the solder bumps 51 is to supply cream solder onto the pads 13 of the carrier substrate 4 by screen printing, and perform heated reflowing, i.e. heating the cream solder at 210° C. if it is eutectic solder of Sn and Pb in a 63/37 weight ratio. The cream solder will then be melted to form the hemispherical solder bumps 51. Another way is to arrange solder balls, so shaped in advance, over the pads 13 and subject them to heated reflowing. Where the space between adjoining pads 13 on the carrier substrate 4 is 1 mm, the pads 13 should desirably be spherical, measuring about 0.5 mm in diameter, and the height of the solder bumps 51 should preferably be 0.5 to 0.7 mm approximately.

Next, the pads 14 on the package bearing substrate 6 and the solder bumps 51 on the carrier substrate 4 are aligned to overlap each other and subjected to heated reflowing so that, as illustrated in FIG. 2B, the pads 13 of the carrier substrate 4 and the pads 14 of the package bearing substrate 6 are electrically and mechanically connected to each other by the solder pieces 5. The size of the pads 14 on the package bearing substrate 6, too, should preferably be substantially equal to that of the pads 13 of the carrier substrate 4. A gap of about 0.5 mm is secured between the carrier substrate 4 and the package bearing substrate 6 by the surface tension of the solder pieces 5. This completes the step to fit the semiconductor package 10 onto the package bearing substrate 6 fitted on the wiring board 9.

Next will be described with reference to a drawing a second preferred embodiment of the present invention, which is characteristic in that a plurality of package bearing substrates are arranged on a wiring board. In other aspects of the configuration, it is the same as the first embodiment.

Referring to FIG. 5, a plurality of package bearing substrates 6 are arranged on a wiring board 91 and, as in the first embodiment, pads 15 on the lower surface of each package bearing substrate 6 are electrically and mechanically connected to pads 161 of the wiring board 91 by solder pieces 82, with the gaps between the package bearing substrates 6 and the wiring board 91 being filled with under-fills 71. Onto each of the package bearing substrates 6 is electrically and mechanically connected one semiconductor package 10 with solder pieces 52.

Next will be described with reference to a drawing a third preferred embodiment of the present invention, which is characteristic in that a plurality of semiconductor packages are mounted on a package bearing substrate on a wiring board. In other aspects of the configuration, it is the same as the first embodiment.

Referring to FIG. 6, onto a package bearing substrate 61 on a wiring board 92, a plurality of semiconductor packages 10 are electrically and mechanically connected by solder

pieces 53. Pads 141 on the package bearing substrate 61 are arranged so that pads 13 of the plurality of semiconductor packages 10 match them, and pads 151 on the lower surface of the package bearing substrate 61 and pads 162 on the wiring board 92 are electrically and mechanically connected by solder pieces 83, and the gap between the package bearing substrate 61 and the wiring board 92 is filled with an under-fill 72 to disperse stresses working on soldered parts and padded parts as described above. However, where the thermal expansion coefficient of the package bearing substrate 61 greatly differs from that of the wiring board 92, for instance where the package bearing substrate 61 is made of alumina and a printed circuit board is used as wiring board 92, if the external dimensions of the package bearing substrate 61 are too great, the stresses will become too severe to be eased by the under-fill 72, possibly causing the under-fill itself to become cracked or come off. Therefore the external dimensions of the package bearing substrate 61 should desirably be at most about 50 mm×50 mm.

Next will be described with reference to a drawing a fourth preferred embodiment of the present invention, which is characteristic in that a plurality of package bearing substrates are mounted on a wiring board, and a plurality of semiconductor packages are mounted on each of said package bearing substrates. In other aspects of the configuration, it is the same as the first embodiment.

Referring to FIG. 7, a plurality of package bearing substrates 61 are arranged on a wiring board 93, and the wiring board 93 and the package bearing substrates 61 are electrically and mechanically connected by solder pieces 84, with the gaps between the wiring board 93 and the package bearing substrates 61 being filled with under-fills 73. On the package bearing substrates 61 are mounted a plurality of semiconductor packages 10 in the same configuration as in the third preferred embodiment of the invention.

As is evident from the foregoing description, according to the present invention, a semiconductor package(s) is (are) mounted by soldering onto a package bearing substrate(s) arranged on a wiring board connected by soldering, with the gap(s) between them filled with an under-fill(s), and the carrier substrate of the semiconductor package(s) and said package bearing substrate(s) are substantially equal or close to each other, with the result that the semiconductor package(s) can be mounted onto the package bearing substrate(s) by direct soldering. It is made possible to arrange soldered terminals at fine spacing, and thereby enable a high density multi-pin mounting structure to be realized.

Furthermore, as said semiconductor package(s) is (are) connected onto said package bearing substrate(s) only by soldering, the semiconductor package(s) can be readily replaced.

What is claimed is:

1. A mounting structure for one or more semiconductor devices comprising:

a wiring board having at least one semiconductor package mounted thereon, said semiconductor package including at least one semiconductor device;

a package bearing substrate whose external size is substantially equal to or larger than that of said semiconductor package and which has first electrodes for connection to said semiconductor package on its upper surface and second electrodes for connection to said wiring board on its lower surface;

solder pieces for connecting third electrodes of said wiring board and said second electrodes on the lower surface of said package bearing substrate, respectively; and

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an under-filling material which fills a gap between said wiring board and said package bearing substrate;

wherein the thermal expansion coefficient of said package bearing substrate arranged on said wiring board is substantially equal to that of said semiconductor package.

2. A mounting structure as claimed in claim 1, wherein a plurality of package bearing substrates are mounted on said wiring board.

3. A mounting structure as claimed in claim 1, wherein one said semiconductor package is connected onto one package bearing substrate on said wiring board by soldering.

4. A mounting structure as claimed in claim 1, wherein a plurality of package bearing substrates are arranged on said wiring board, and one said semiconductor package is connected to one package bearing substrate by soldering.

5. A mounting structure as claimed in claim 1, wherein a plurality of said semiconductor packages are connected to one package bearing substrate on said wiring board by soldering.

6. A mounting structure as claimed in claim 1, wherein a plurality of package bearing substrates are arranged on said

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wiring board, and a plurality of said semiconductor packages are connected to one package bearing substrate by soldering.

7. A mounting structure as claimed in claim 3, wherein the difference between the thermal expansion coefficient of the package bearing substrate arranged on said wiring board and that of said semiconductor package is not more than 50% of the thermal expansion coefficient of said semiconductor package.

8. A mounting structure as claimed in claim 3, wherein the melting point of the solder connecting said wiring board and the package bearing substrate arranged on said wiring board is equal to that of the solder connecting said package bearing substrate and said semiconductor package.

9. A mounting structure as claimed in claim 3, wherein the melting point of the solder connecting said wiring board and the package bearing substrate arranged on said wiring board is higher than that of the solder connecting said package bearing substrate and said semiconductor package.

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